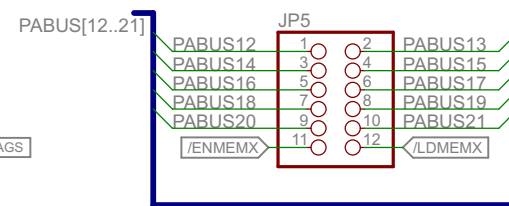
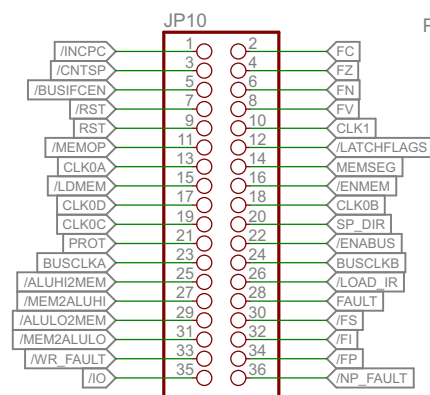
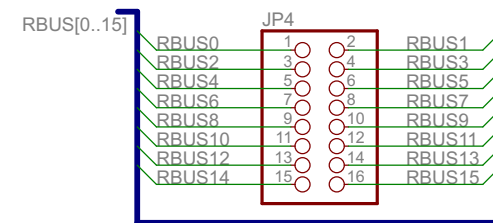
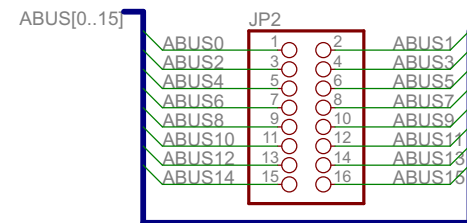
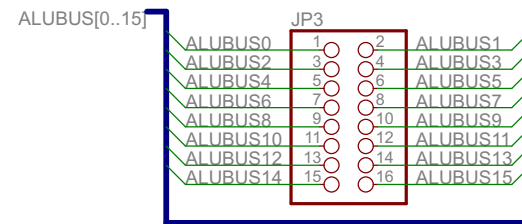
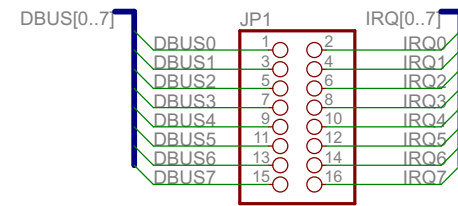
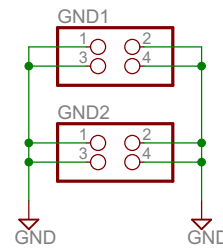
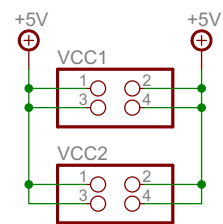
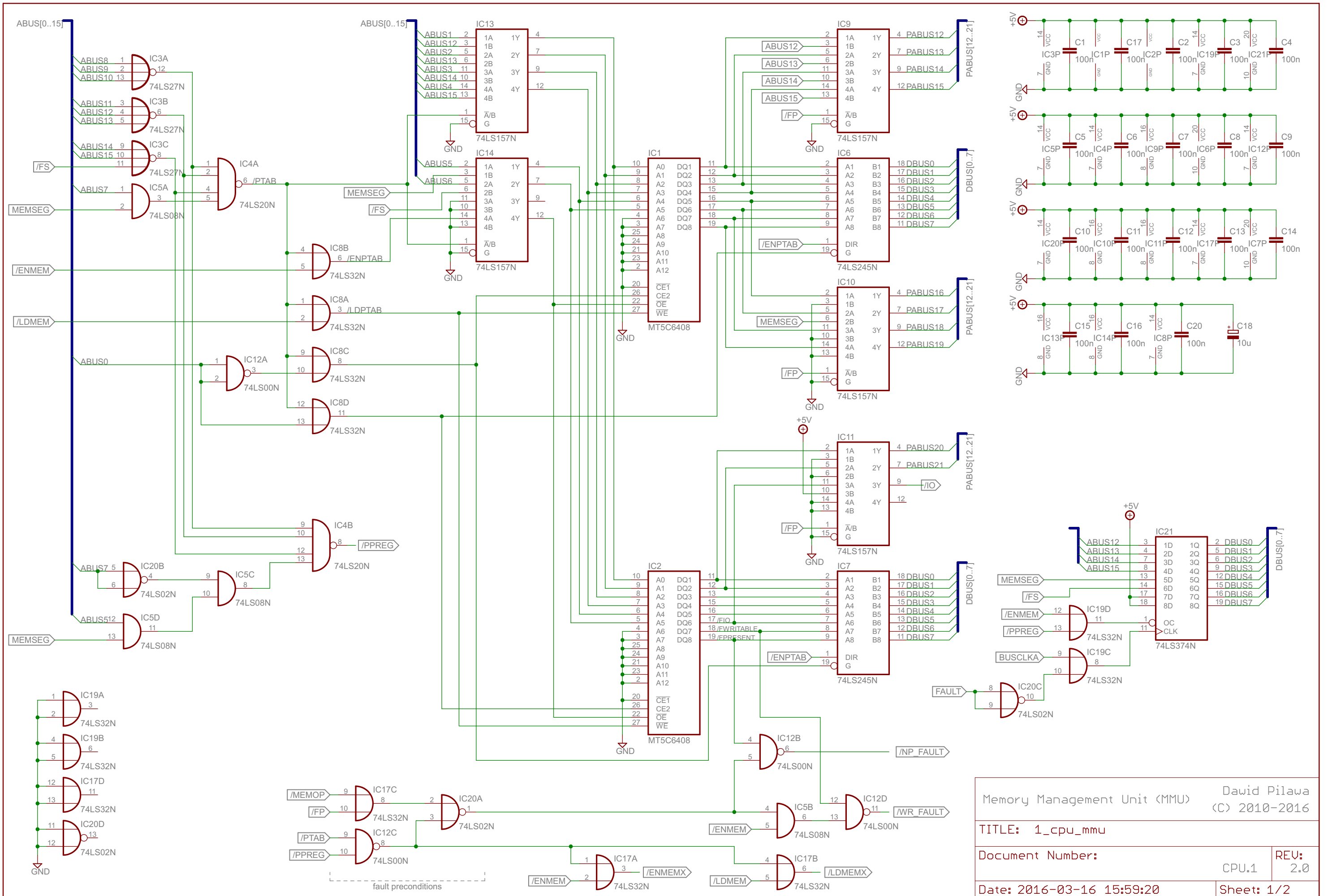


Clocks, reset, bus interface		Dawid Pilawa (C) 2010-2016	
TITLE: 0_cpu_interface			
Document Number:		CPU.0	REV: 2.0
Date: 2016-02-12 16:16:01		Sheet: 1/2	

BOARD CONNECTORS

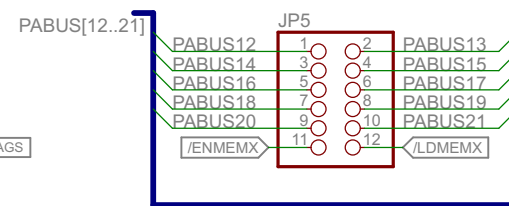
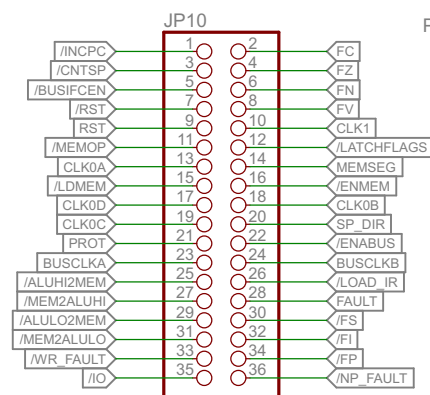
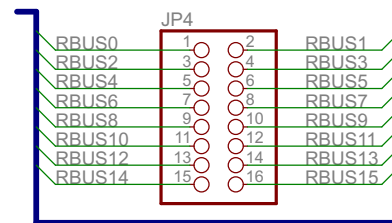
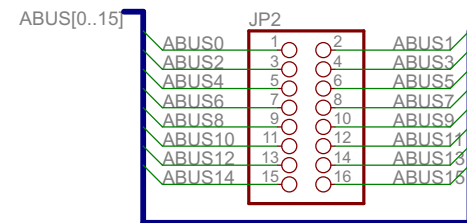
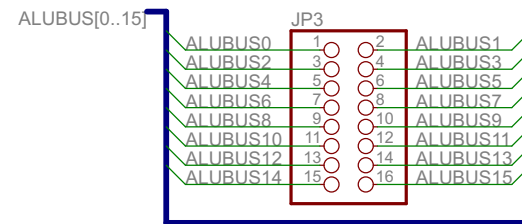
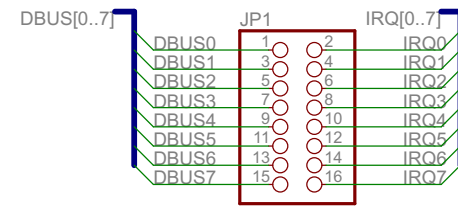
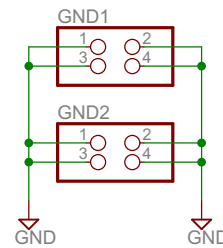
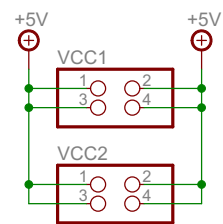


Clocks, reset, bus interface		Dawid Pilawa (C) 2010-2016	
TITLE: 0_cpu_interface			
Document Number:		CPU.0	REV: 2.0
Date: 2016-02-12 16:16:01		Sheet: 2/2	

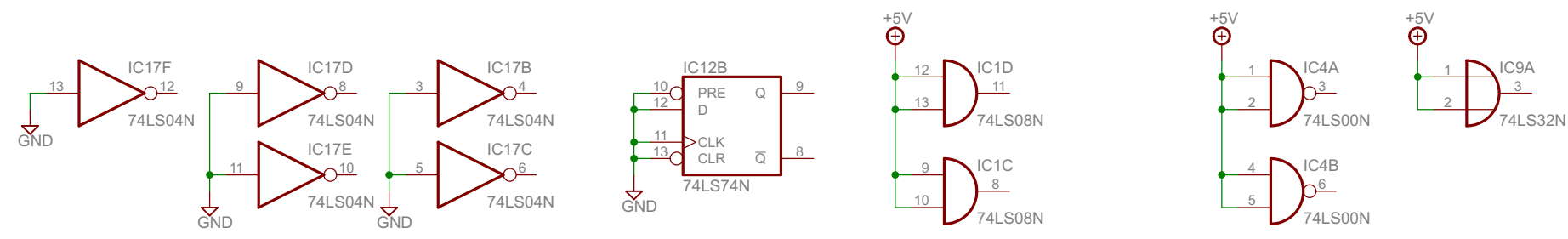
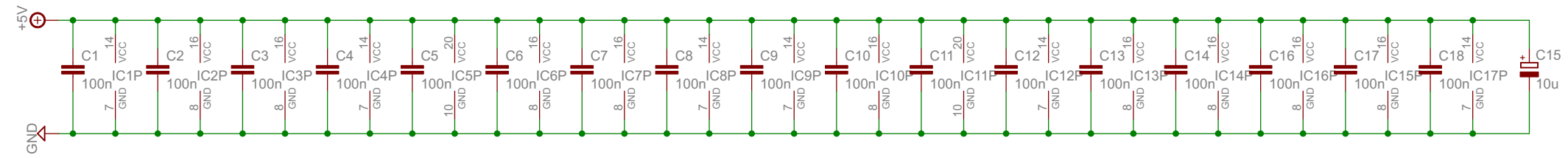
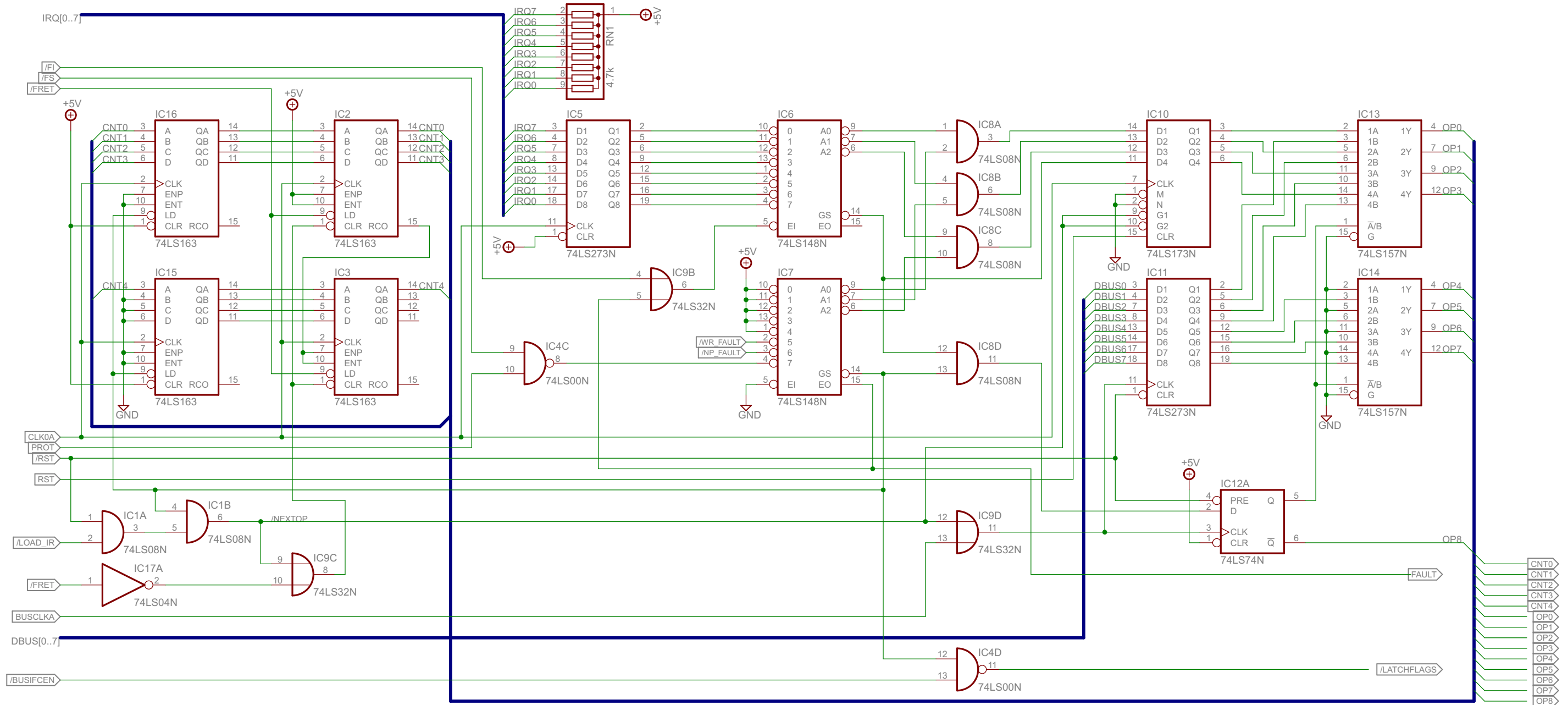


Memory Management Unit (MMU)		Dawid Pilawa	
		(C) 2010-2016	
TITLE: 1_cpu_mmu			
Document Number:		CPU.1	REV: 2.0
Date: 2016-03-16 15:59:20		Sheet: 1/2	

BOARD CONNECTORS

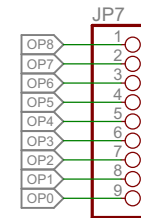
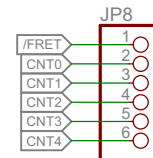
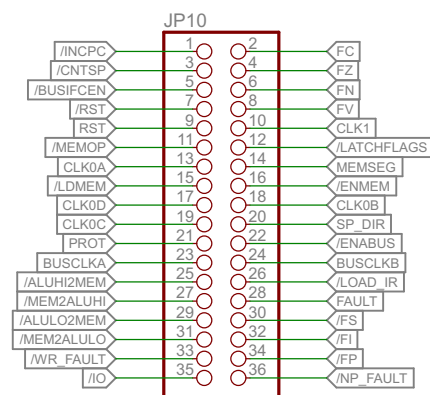
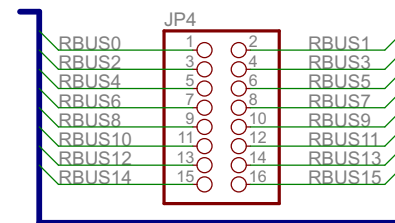
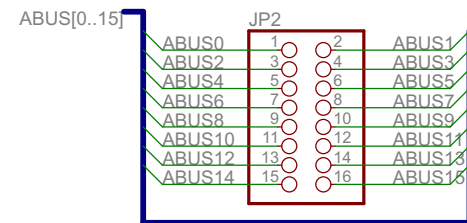
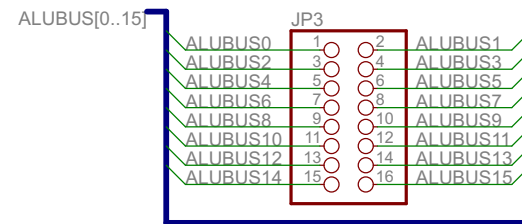
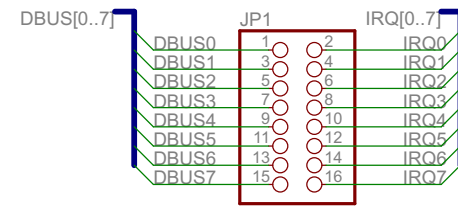
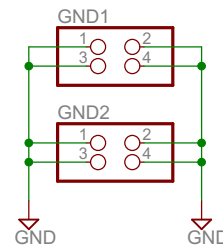
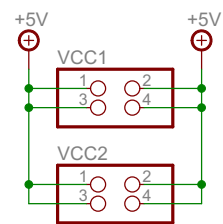


Memory Management Unit (MMU)		Dawid Pilawa (C) 2010-2014	
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Document Number:		CPU.1	REV: 2.0
Date: 2016-03-16 15:59:20			Sheet: 2/2

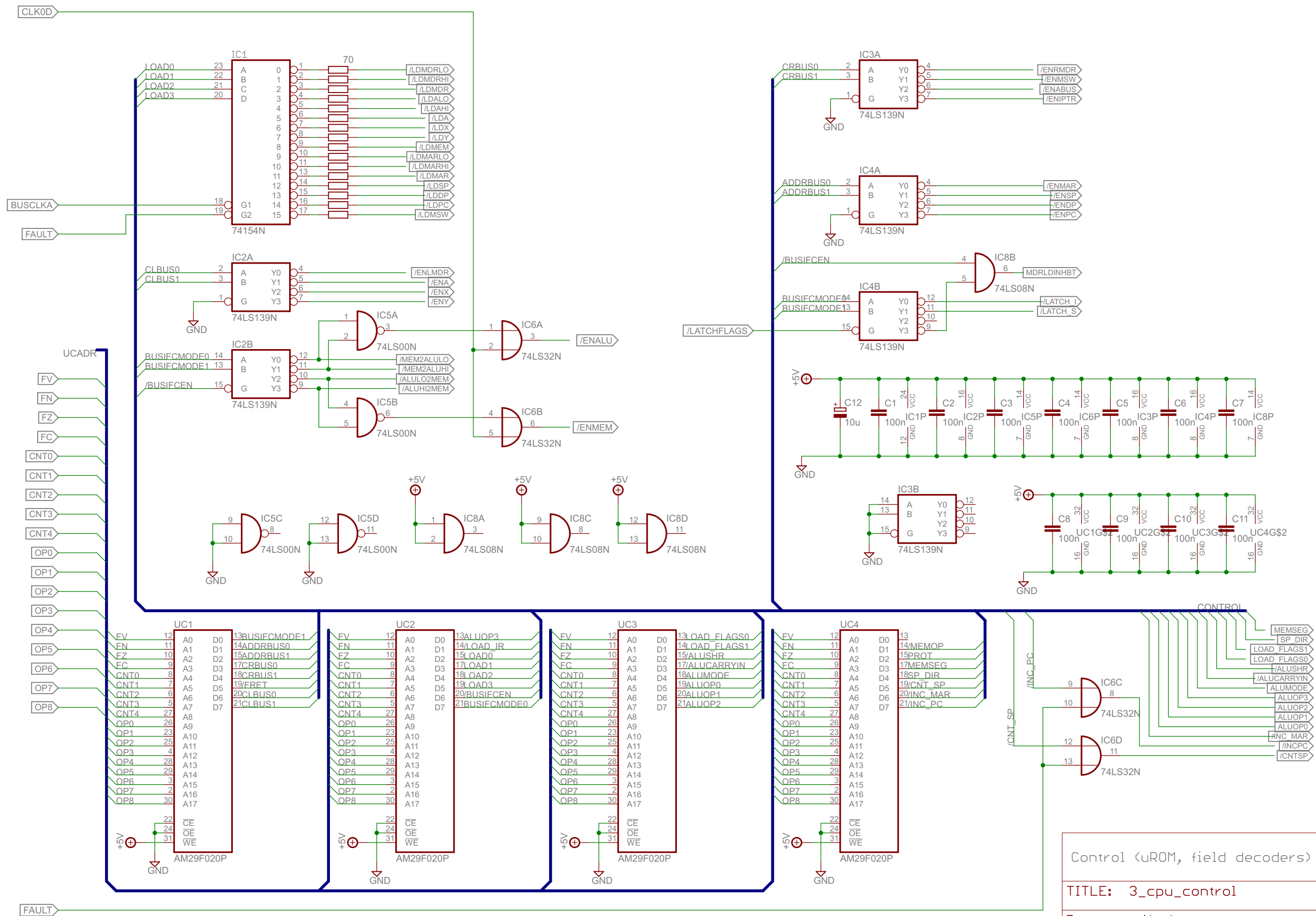


Control (microcode sequencer)		Dawid Pilawa	
		(C) 2010-2016	
TITLE: 2_cpu_control			
Document Number:		CPU.2	REV: 2.0
Date: 2016-02-19 17:32:08			Sheet: 1/2

BOARD CONNECTORS

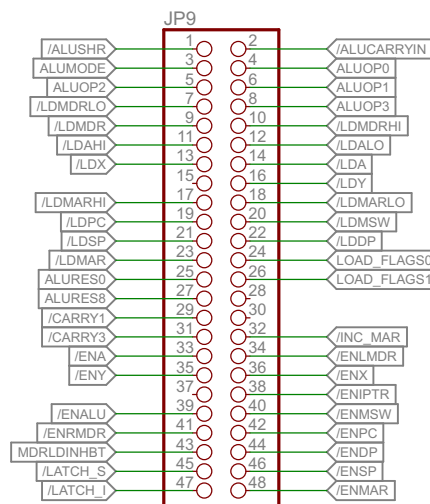
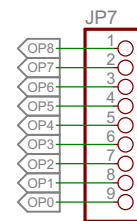
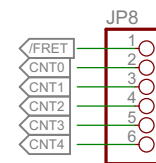
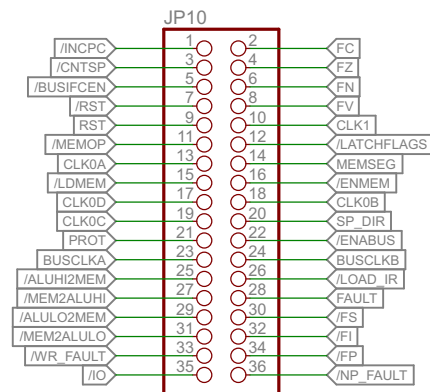
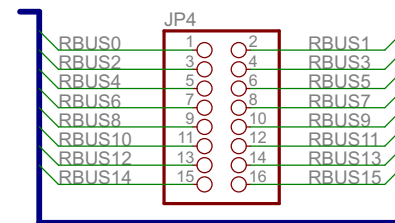
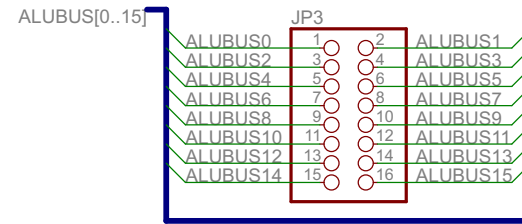
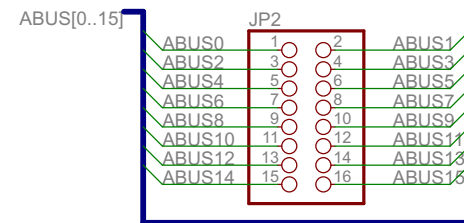
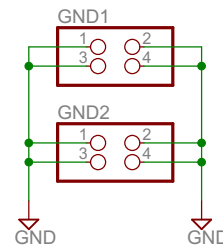
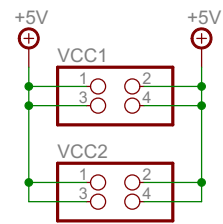


Control (microcode sequencer)		Dawid Pilawa (C) 2010-2016	
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Document Number:		CPU.2	REV: 2.0
Date: 2016-02-19 17:32:08		Sheet: 2/2	

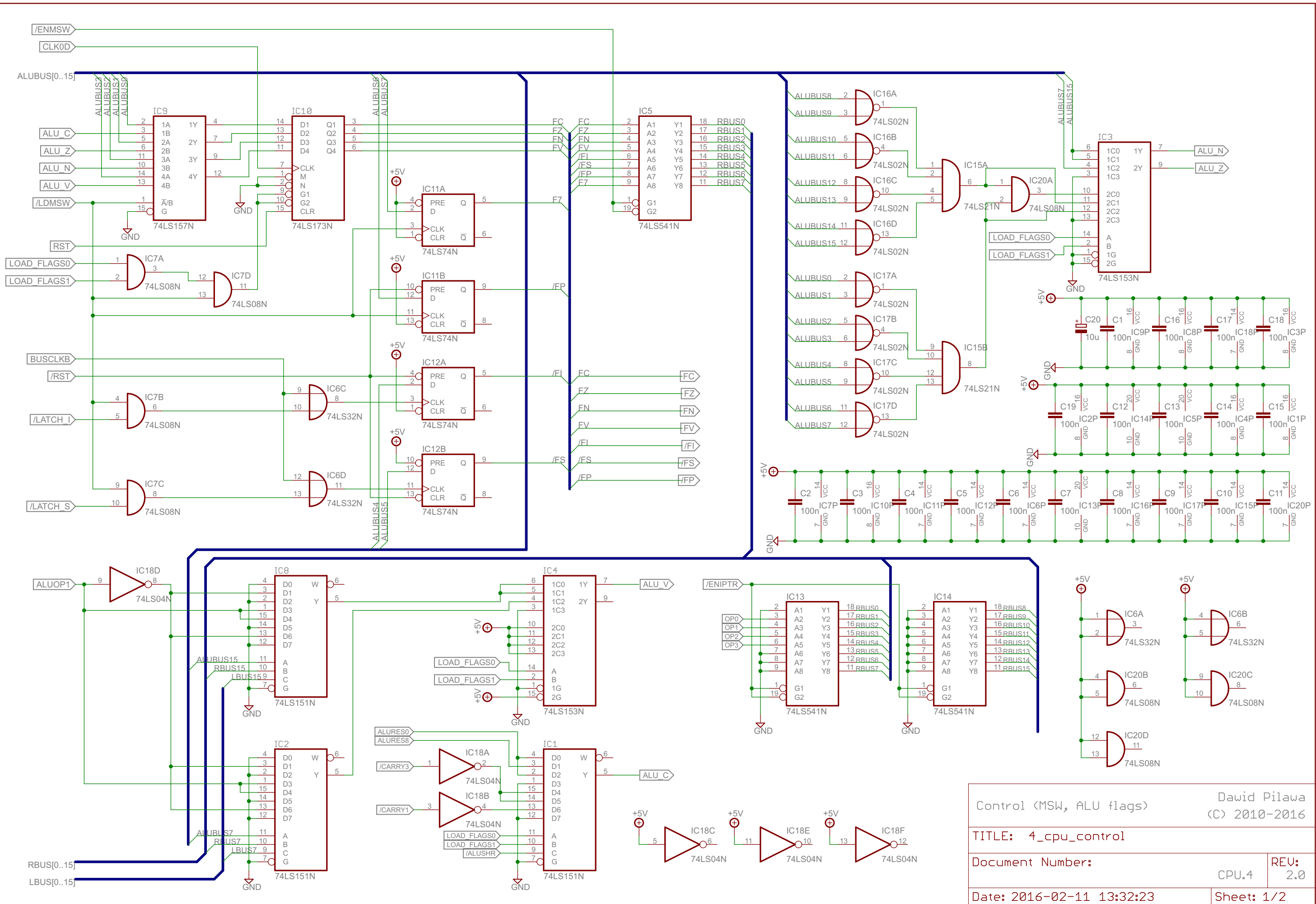


Control (uROM, field decoders)		Dawid Pilawa (C) 2010-2016	
TITLE: 3_cpu_control			
Document Number:		CPU.3	REV: 2.0
Date: 2016-02-12 16:16:01		Sheet: 1/2	

BOARD CONNECTORS

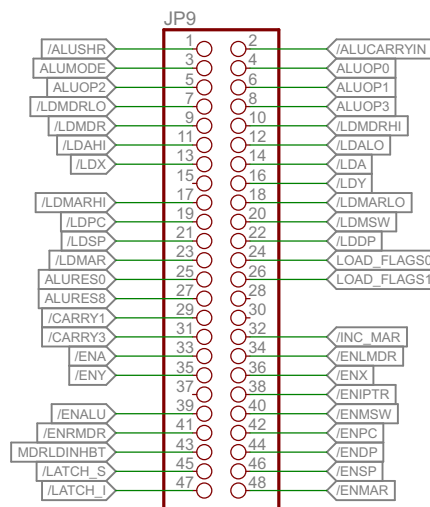
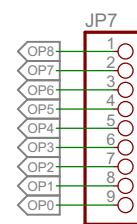
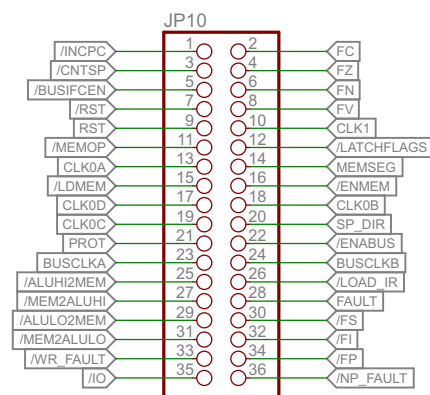
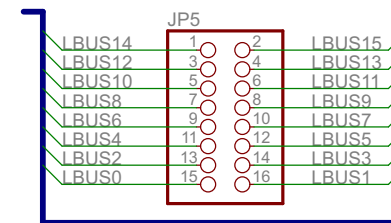
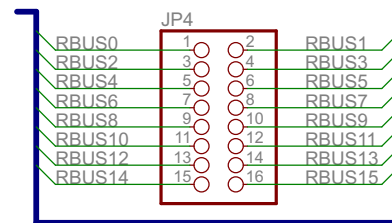
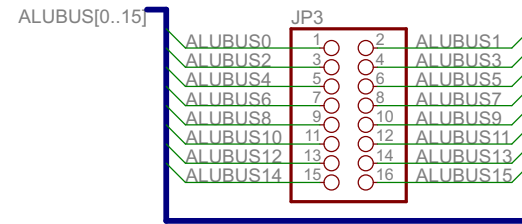
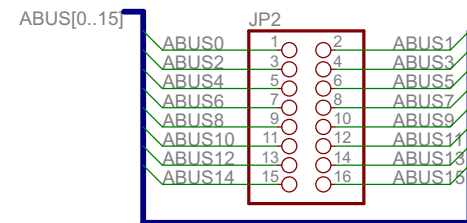
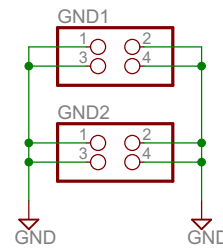
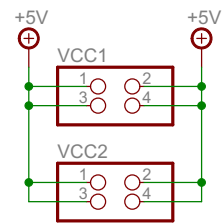


Control (uROM, field decoders)		Dawid Pilawa (C) 2010-2016	
TITLE: 3_cpu_control			
Document Number:		CPU.3	REV: 2.0
Date: 2016-02-12 16:16:01		Sheet: 2/2	

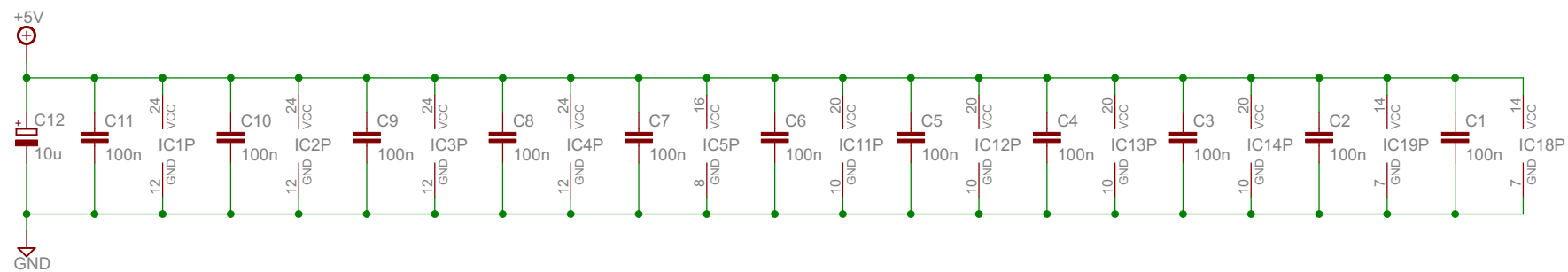
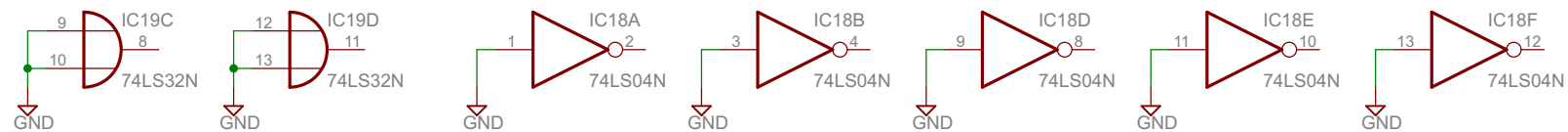
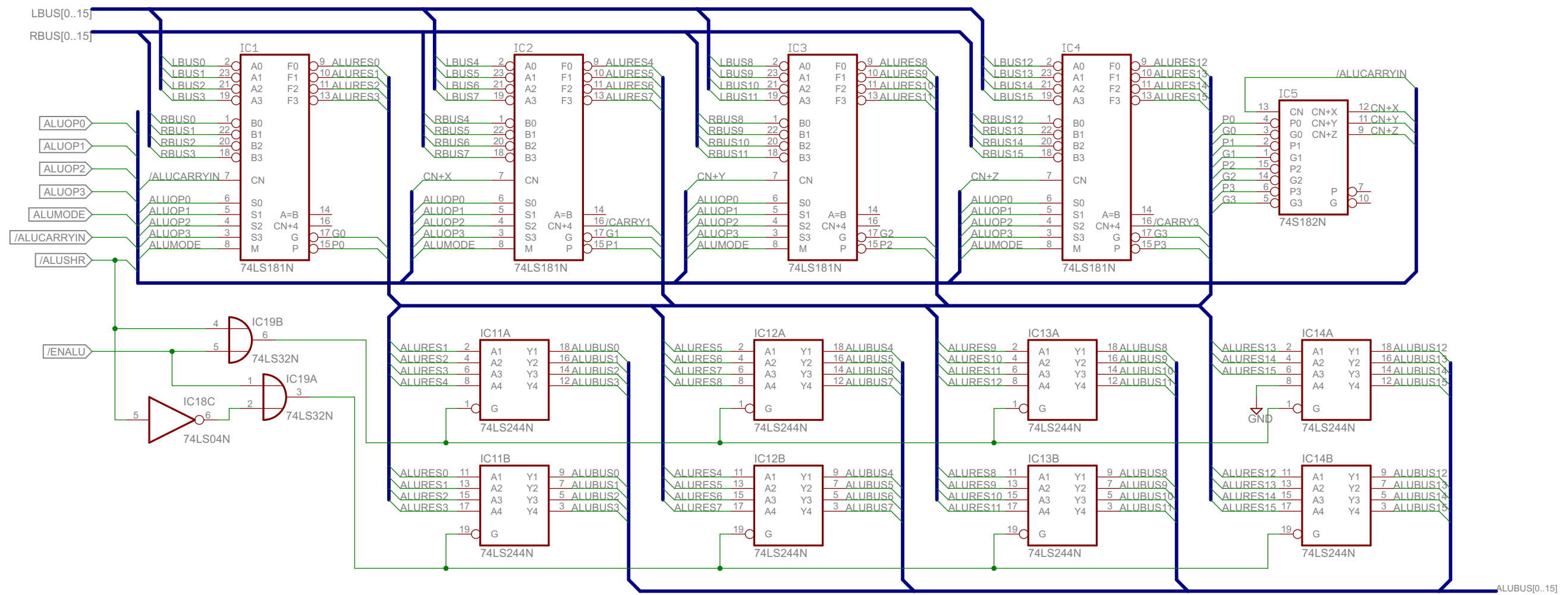


Control (MSW, ALU flags)		Dawid Pilawa (C) 2010-2016	
TITLE: 4_cpu_control			
Document Number:		CPU.4	REV: 2.0
Date: 2016-02-11 13:32:23		Sheet: 1/2	

BOARD CONNECTORS

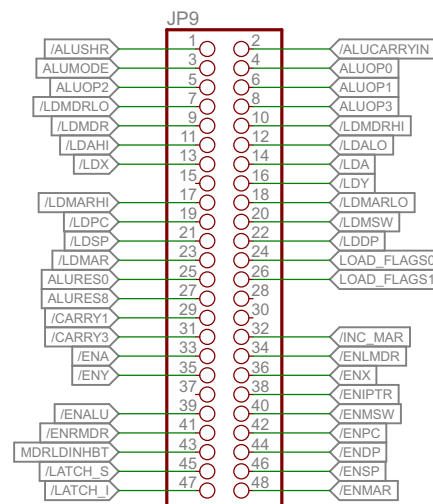
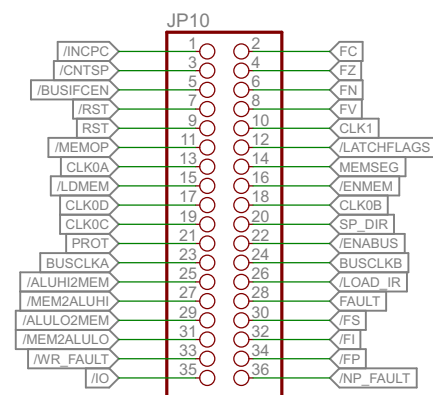
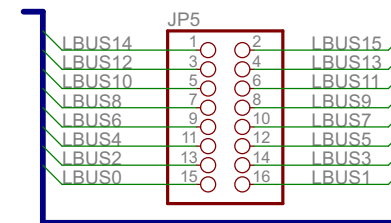
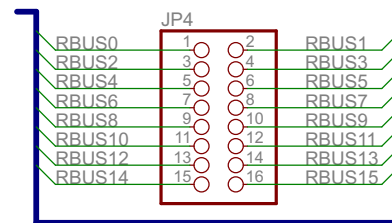
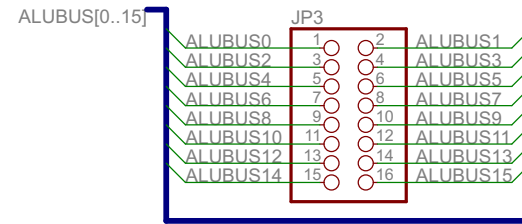
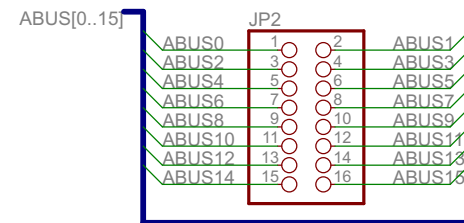
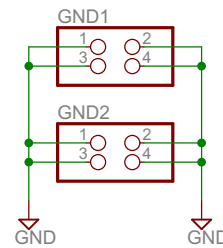
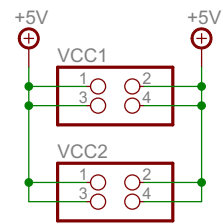


Control (MSW, ALU flags)		Dawid Pilawa (C) 2010-2016	
TITLE: 4_cpu_control			
Document Number:		CPU.4	REV: 2.0
Date: 2016-02-11 13:32:23		Sheet: 2/2	



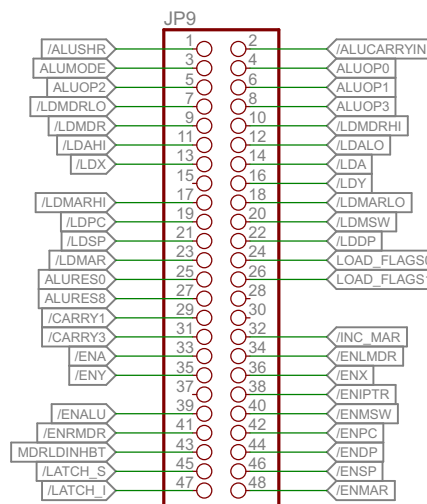
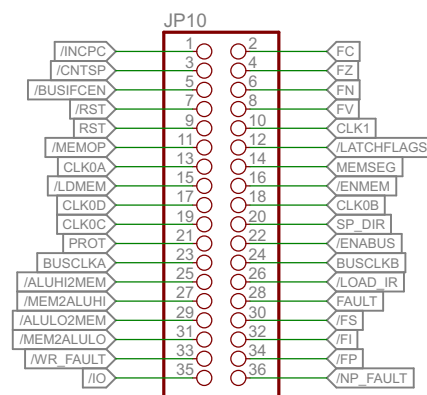
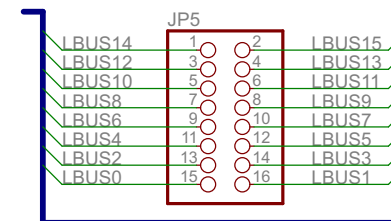
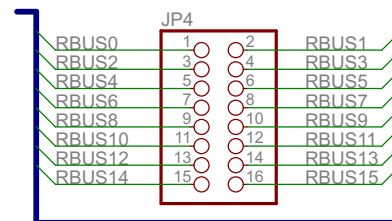
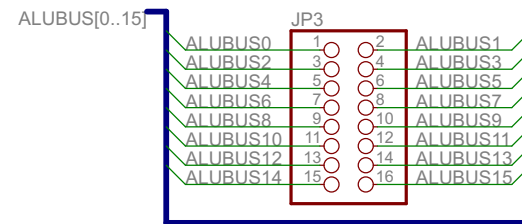
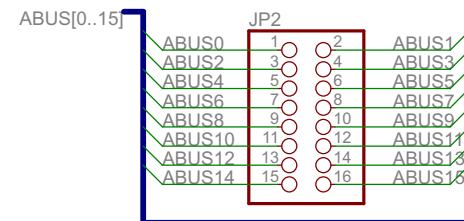
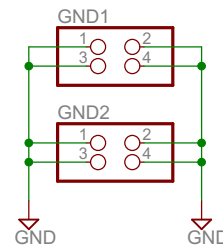
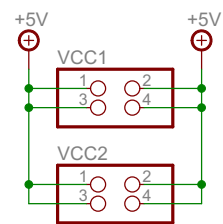
Arithmetic Logic Unit (ALU)		Dawid Pilawa	
		(C) 2010-2016	
TITLE: 5_cpu_alu			
Document Number:		CPU.5	REV: 2.0
Date: 2016-02-11 13:32:23		Sheet: 1/2	

BOARD CONNECTORS

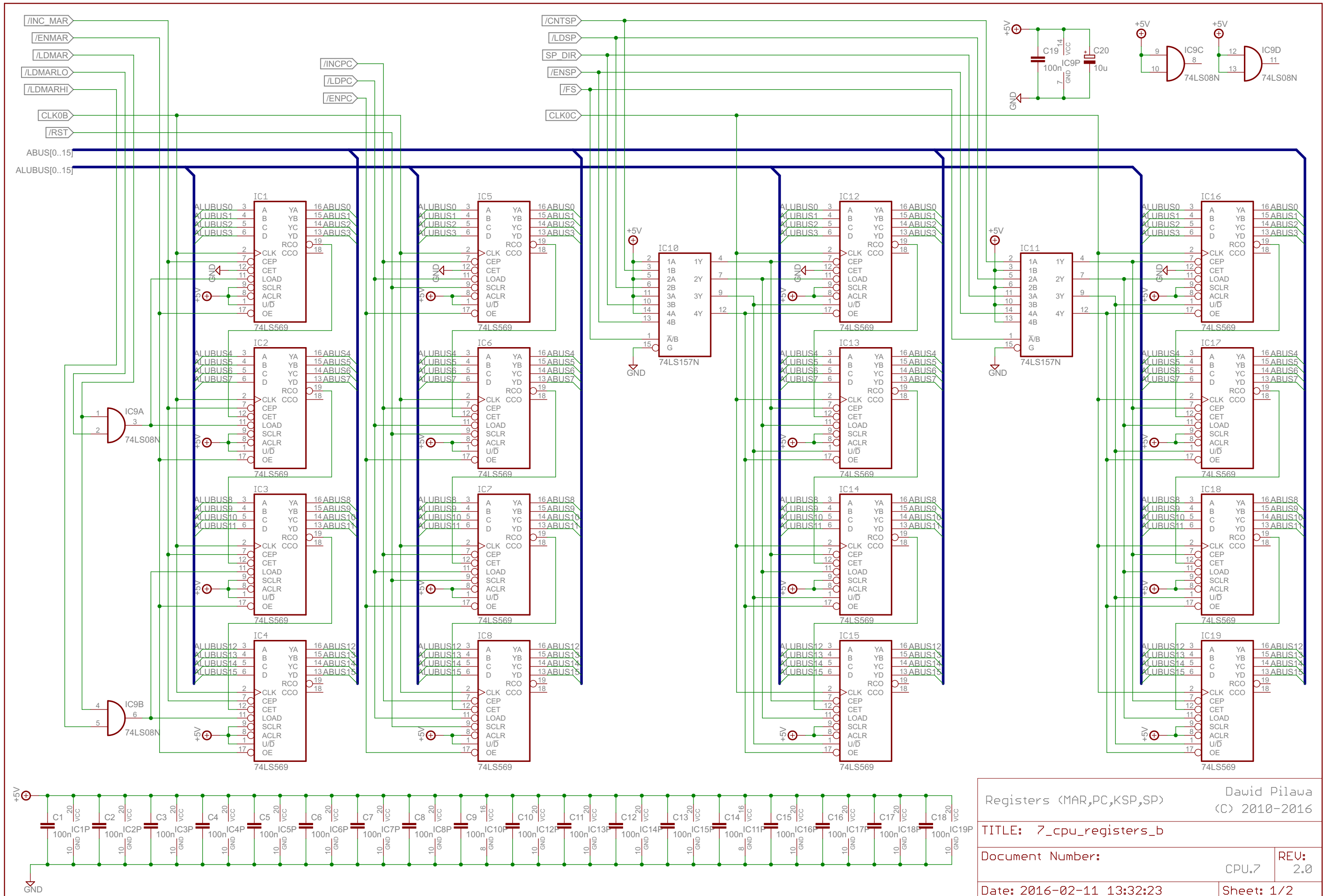


Arithmetic Logic Unit (ALU)		Dawid Pilawa (C) 2010-2016	
TITLE: 5_cpu_alu			
Document Number:		CPU.5	REV: 2.0
Date: 2016-02-11 13:32:23		Sheet: 2/2	

BOARD CONNECTORS

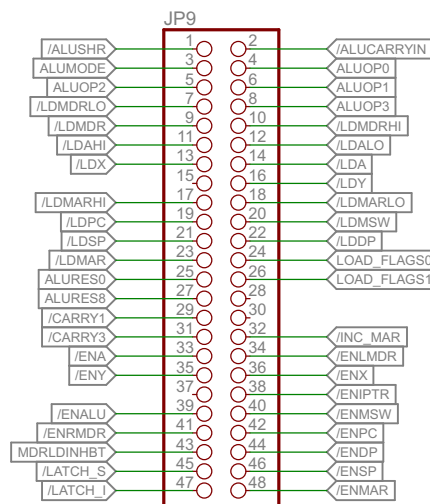
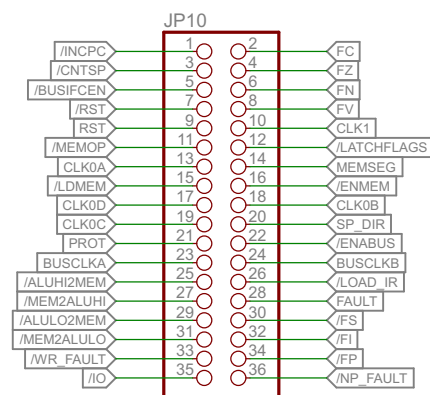
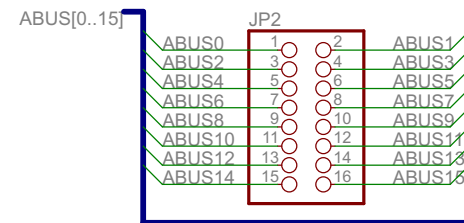
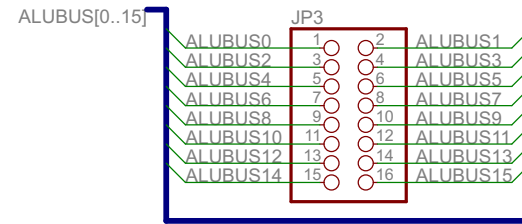
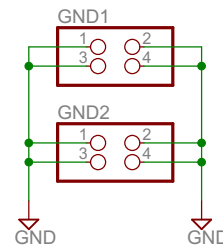
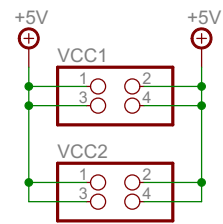


Registers (MDR,DP,A,X,Y)		Dawid Pilawa (C) 2010-2016	
TITLE: 6_cpu_registers_a			
Document Number:		CPU.6	REV: 2.0
Date: 2016-02-11 13:32:23		Sheet: 2/2	

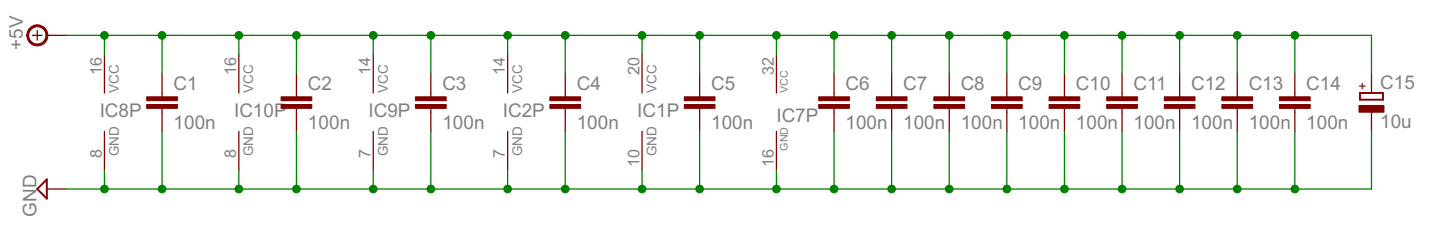
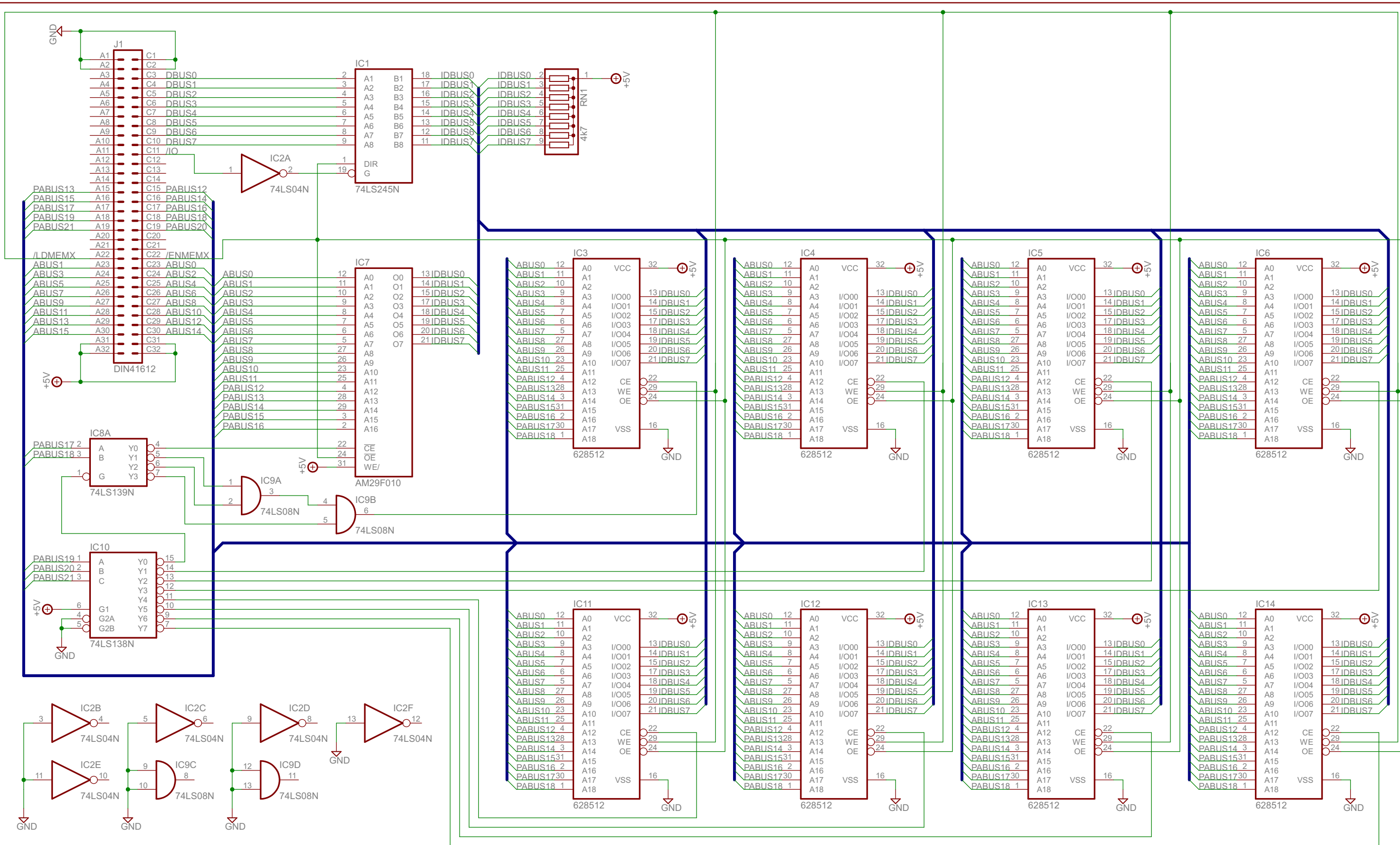


Registers (MAR,PC,KSP,SP) Dawid Pilawa
 (C) 2010-2016
 TITLE: 7_cpu_registers_b
 Document Number: CPU.7 REV: 2.0
 Date: 2016-02-11 13:32:23 Sheet: 1/2

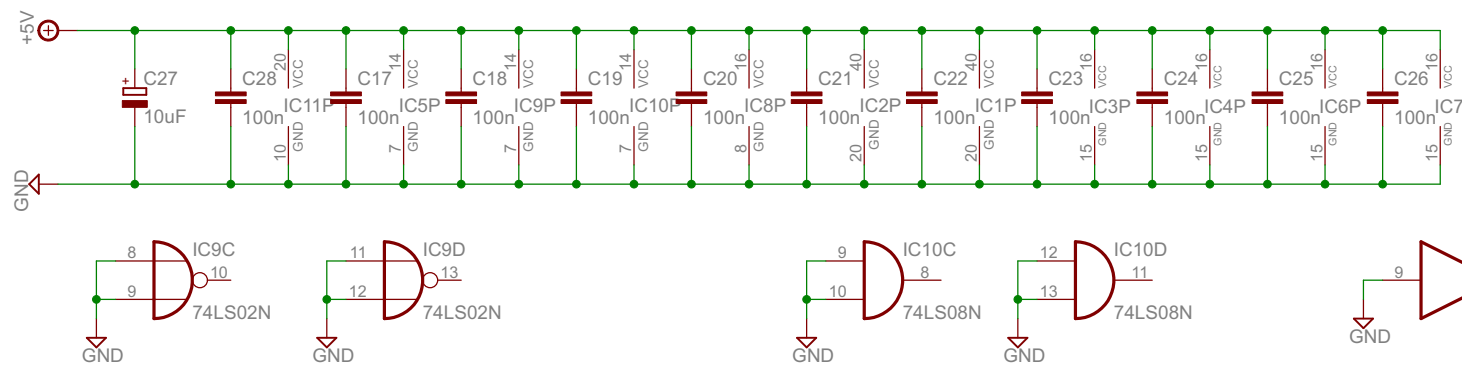
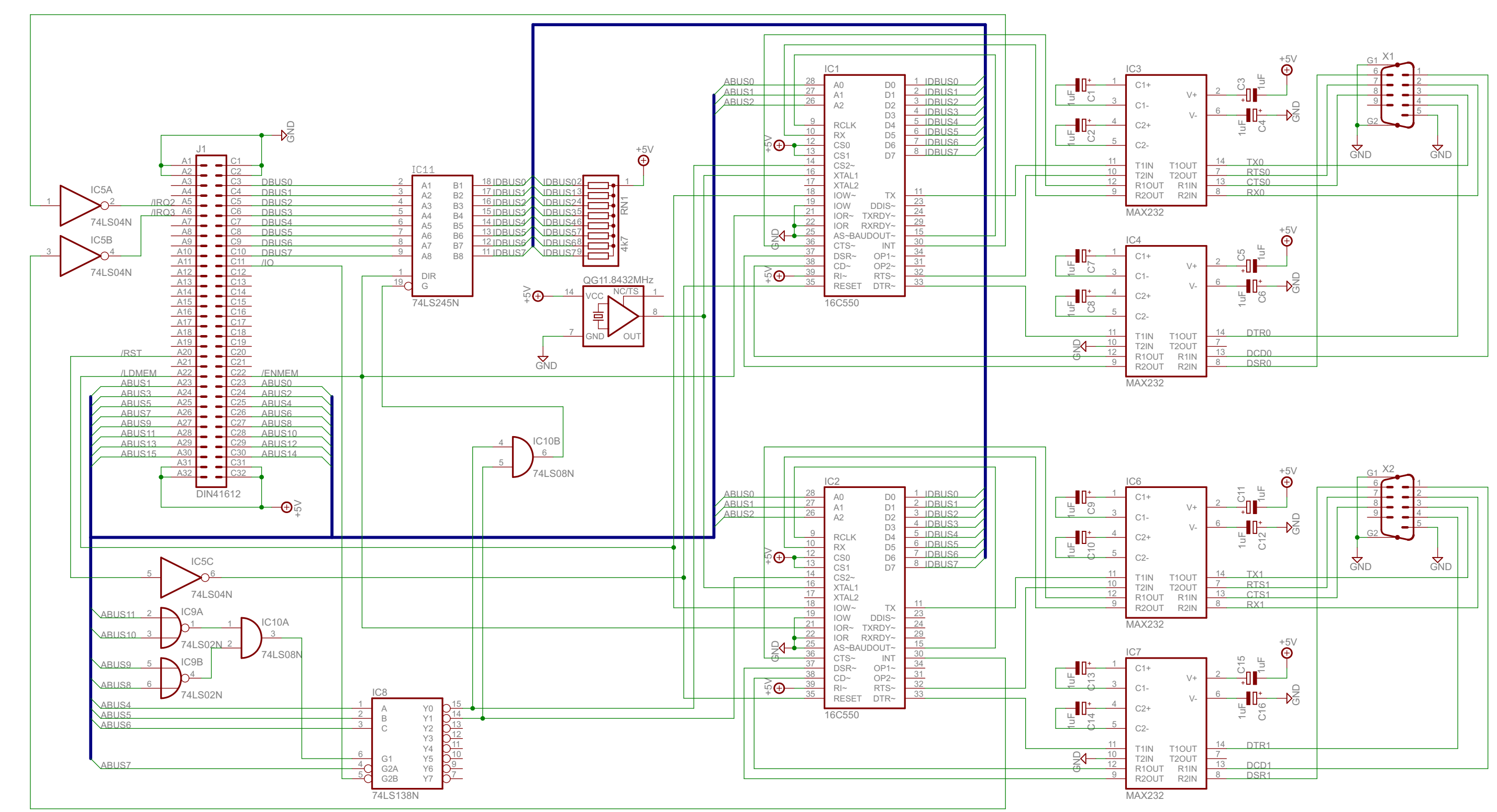
BOARD CONNECTORS



Registers (MAR,PC,KSP,SP)	Dawid Pilawa (C) 2010-2016
TITLE: 7_cpu_registers_b	
Document Number:	REU: 2.0
Date: 2016-02-11 13:32:23	CPU.7 Sheet: 2/2



Memory (ROM & RAM)		Dawid Pilawa (C) 2010-2016	
TITLE: memory			
Document Number:		MEM.1	REV: 2.0
Date: 2016-03-03 17:42:55		Sheet: 1/1	



I/O - UARTS		Dawid Pilawa	
		(C) 2010 - 2012	
TITLE: io_uartS			
Document Number:		REV: 1.0.3	
		10.1	
Date: 2016-02-11 13:32:24		Sheet: 1/1	

