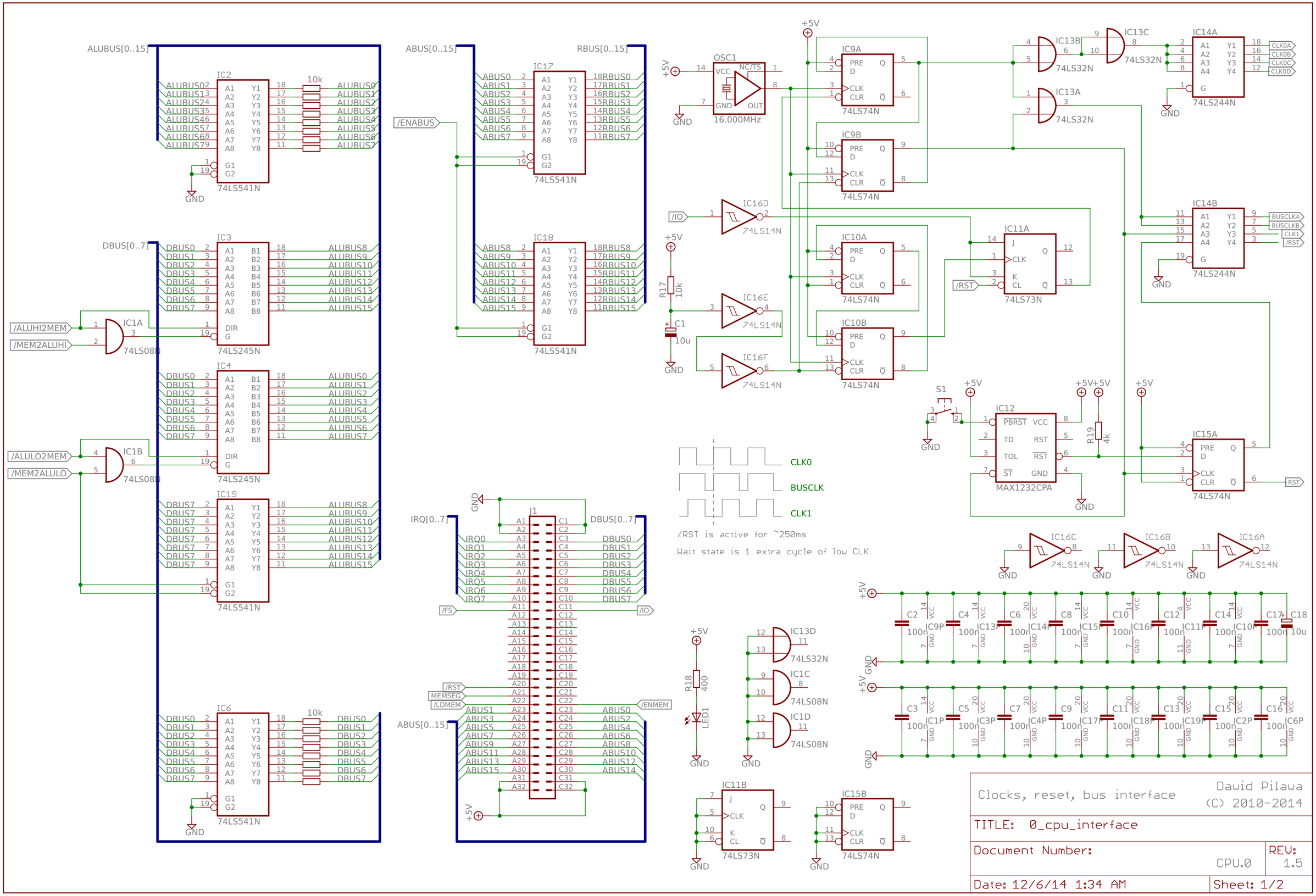
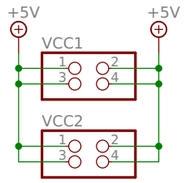
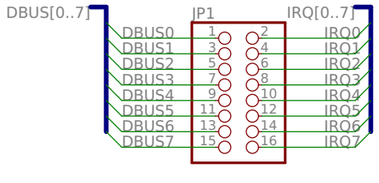
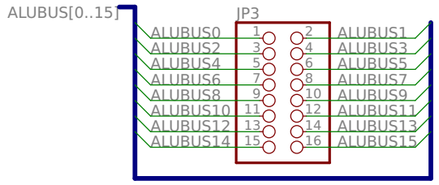
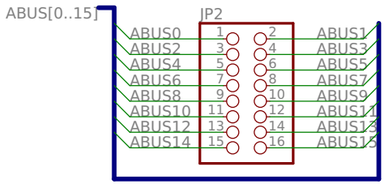

ALUBUS[0..15]
IC2
10k
74LS541N
GND
DBUS[0..7]
IC3
74LS245N
/ALUHI2MEM
/MEM2ALUHI
IC1A
74LS08N
IC4
/ALULO2MEM
/MEM2ALULO
IC1B
IC19
IC6
ABUS[0..15]
RBUS[0..15]
/ENABUS
IC17
IC18
IRQ[0..7]
J1
/FS
/IO
/RST
MEMSEG
/LDMEM
/ENMEM
+5V
OSC1
16.000MHz
IC9A
IC9B
74LS74N
IC16D
IC16E
IC16F
74LS14N
R17
10k
C1
10u
IC10A
IC10B
IC11A
74LS73N
/RST
IC13B
IC13C
74LS32N
IC13A
IC14A
IC14B
74LS244N
CLK0A
CLK0B
CLK0C
CLK0D
BUSCLKA
BUSCLKB
CLK1
/RST
S1
IC12
MAX1232CPA
R19
4k
IC15A
74LS74N
CLK0
BUSCLK
CLK1
/RST is active for ~250ms
Wait state is 1 extra cycle of low CLK
IC16C
IC16B
IC16A
IC13D
IC1C
IC1D
74LS08N
R18
400
LED1
IC11B
IC15B
C2
C4
C6
C8
C10
C12
C14
C17
C18
C3
C5
C7
C9
C11
C13
C15
C16
100n
10u
Clocks, reset, bus interface
Dawid Pilawa
(C) 2010-2014
TITLE: 0_cpu_interface
Document Number:
CPU.0
REV:
1.5
Date: 12/6/14 1:34 AM
Sheet: 1/2

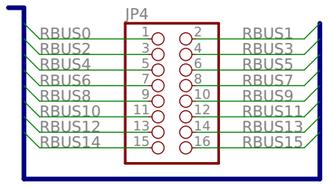
# BOARD CONNECTORS

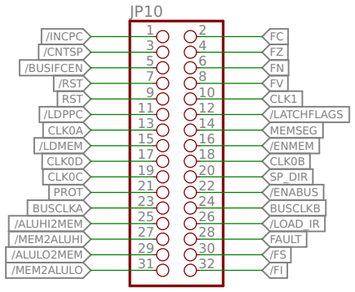


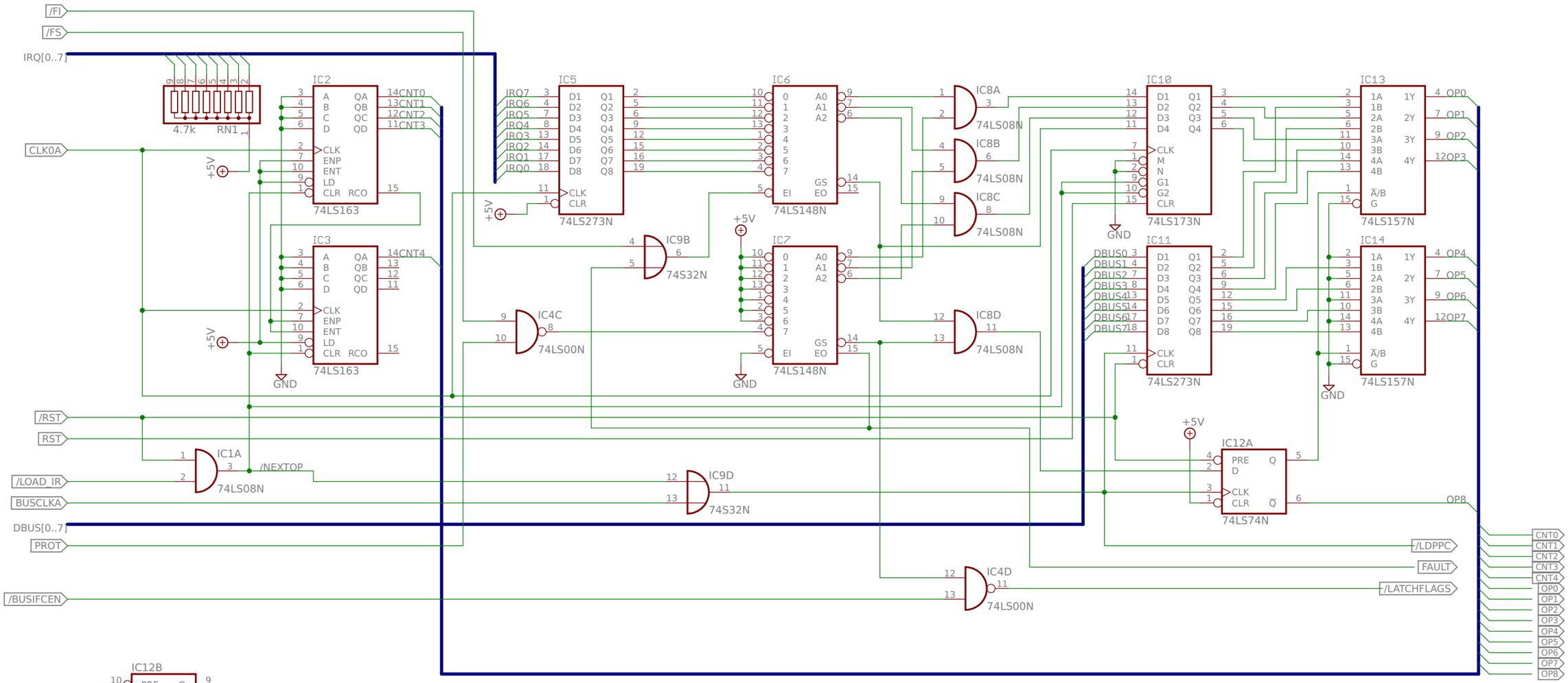




| | |
|---|---|
| Clocks, reset, bus interface | Dawid Pilawa<br>(C) 2010-2014 |
| TITLE: 0_cpu_interface | |
| Document Number: CPU.0 | REV: 1.5 |
| Date: 12/6/14 1:34 AM | Sheet: 2/2 |




Control (ucode sequencer)

Dawid Pilawa
(C) 2010-2014

TITLE: 1_cpu_control

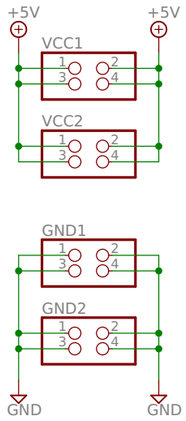
Document Number: CPU.1

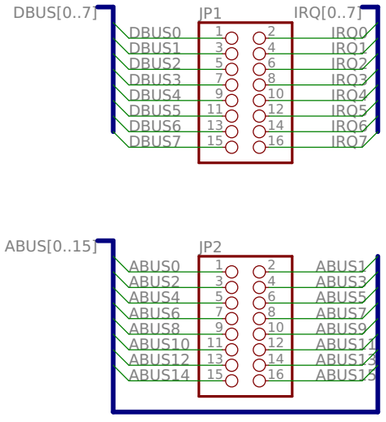
REV: 1.5

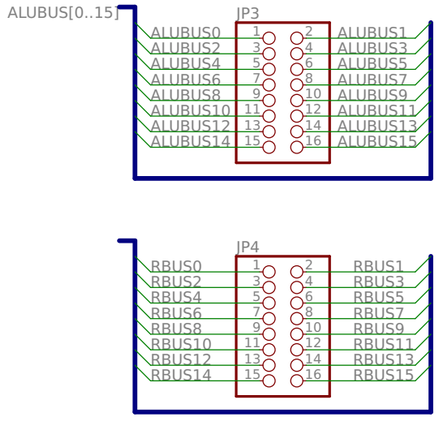
Date: 12/6/14 1:34 AM

Sheet: 1/2

# BOARD CONNECTORS



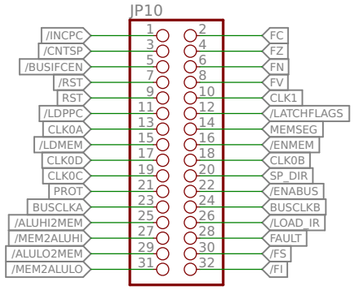



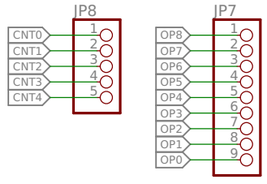









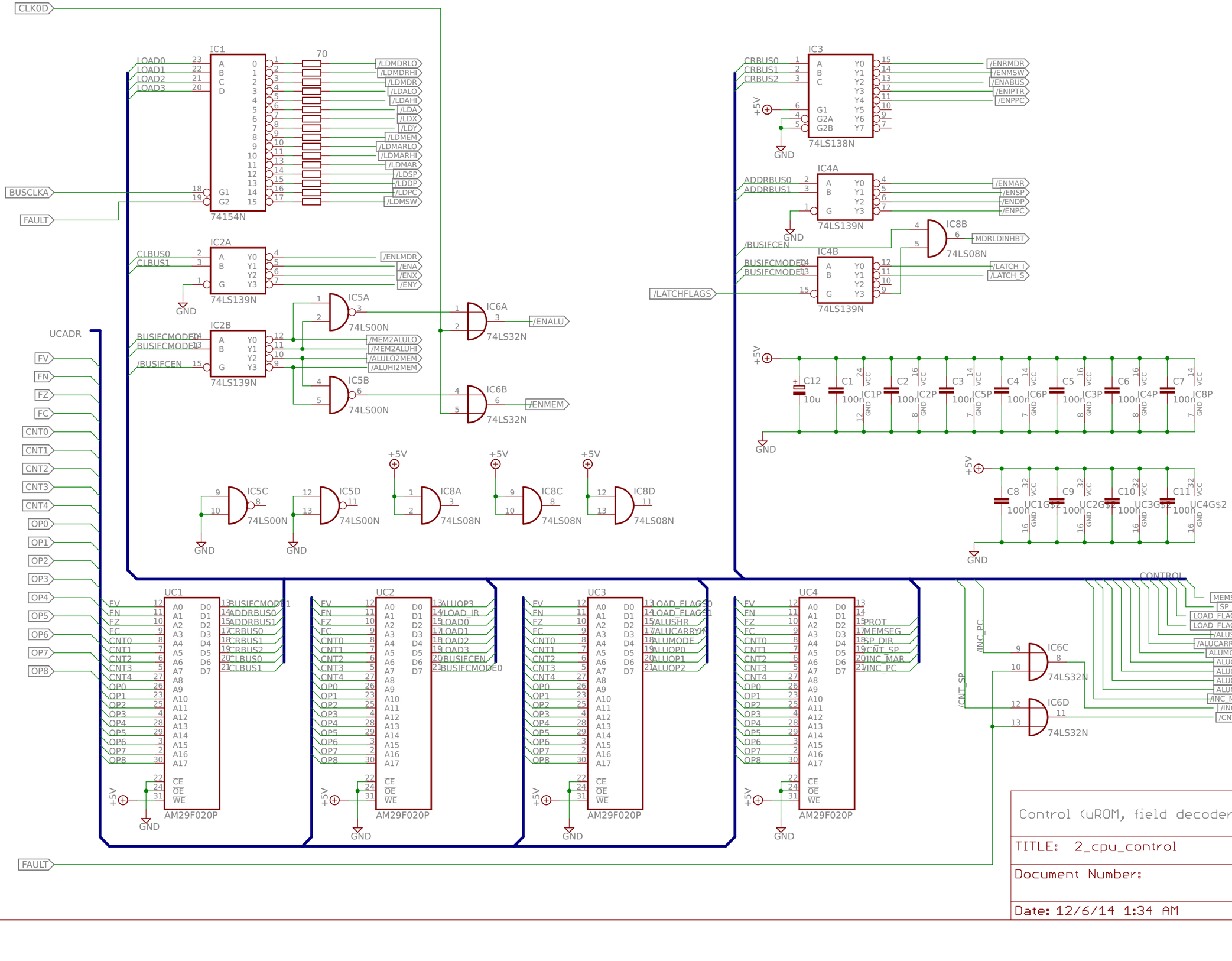



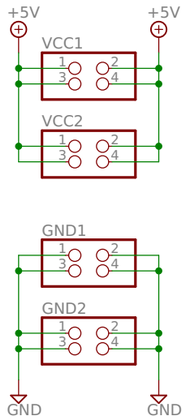


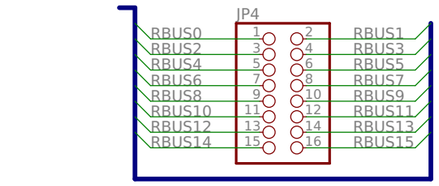


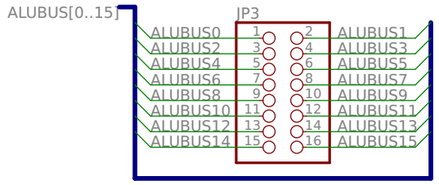
| | |
|---|---|
| Control (ucode sequencer) | Dawid Pilawa<br>(C) 2010-2014 |
| TITLE: 1_cpu_control | |
| Document Number: CPU.1 | REV: 1.5 |
| Date: 12/6/14 1:34 AM | Sheet: 2/2 |


CLK0D
IC1
LOAD0
LOAD1
LOAD2
LOAD3
BUSCLKA
FAULT
74154N
70
/LDMDRLO
/LDMDRHI
/LDMDR
/LDALO
/LDAHI
/LDA
/LDX
/LDY
/LDMEM
/LDMARLO
/LDMARHI
/LDMAR
/LDSP
/LDDP
/LDPC
/LDMSW
IC2A
CLBUS0
CLBUS1
74LS139N
GND
/ENLMDR
/ENA
/ENX
/ENY
IC2B
BUSIFCMODE1
BUSIFCMODE0
/BUSIFCEN
/MEM2ALULO
/MEM2ALUHI
/ALULO2MEM
/ALUHI2MEM
IC5A
74LS00N
IC5B
IC6A
74LS32N
/ENALU
IC6B
/ENMEM
UCADR
FV
FN
FZ
FC
CNT0
CNT1
CNT2
CNT3
CNT4
OP0
OP1
OP2
OP3
OP4
OP5
OP6
OP7
OP8
+5V
IC5C
IC5D
IC8A
IC8C
IC8D
74LS08N
IC3
CRBUS0
CRBUS1
CRBUS2
74LS138N
/ENRMDR
/ENMSW
/ENABUS
/ENIPTR
/ENPPC
IC4A
ADDRBUS0
ADDRBUS1
/ENMAR
/ENSP
/ENDP
/ENPC
IC4B
/LATCHFLAGS
IC8B
MDRLDINHBT
/LATCH_I
/LATCH_S
C12
10u
C1
C2
C3
C4
C5
C6
C7
100n
C1P
C2P
C3P
C4P
C5P
C6P
C8P
VCC
C8
C9
C10
C11
UC1G$2
UC2G$2
UC3G$2
UC4G$2
UC1
UC2
UC3
UC4
AM29F020P
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
D0
D1
D2
D3
D4
D5
D6
D7
CE
OE
WE
ALUOP3
/LOAD_IR
LOAD0
LOAD1
LOAD2
LOAD3
BUSIFCEN
BUSIFCMODE0
LOAD_FLAGS0
LOAD_FLAGS1
ALUSHR
ALUCARRYIN
ALUMODE
ALUOP0
ALUOP1
ALUOP2
PROT
MEMSEG
SP_DIR
/CNT_SP
/INC_MAR
/INC_PC
CONTROL
/INC_PC
/CNT_SP
IC6C
IC6D
/INCPC
/CNTSP
FAULT
Control (uROM, field decoders)
Dawid Pilawa
(C) 2010-2014
TITLE: 2_cpu_control
Document Number:
CPU.2
REV:
1.5
Date: 12/6/14 1:34 AM
Sheet: 1/2

# BOARD CONNECTORS

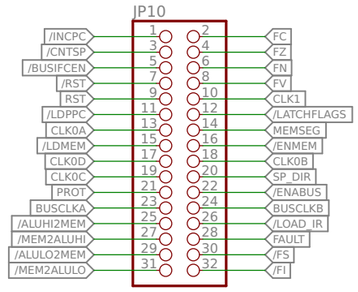


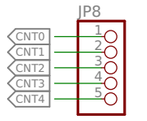



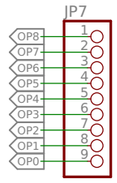



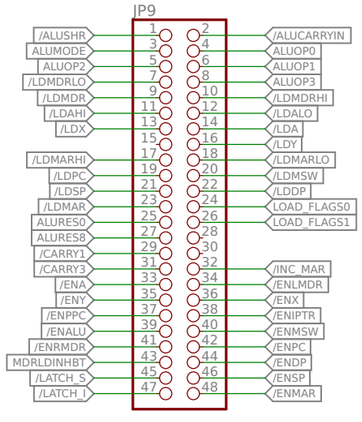




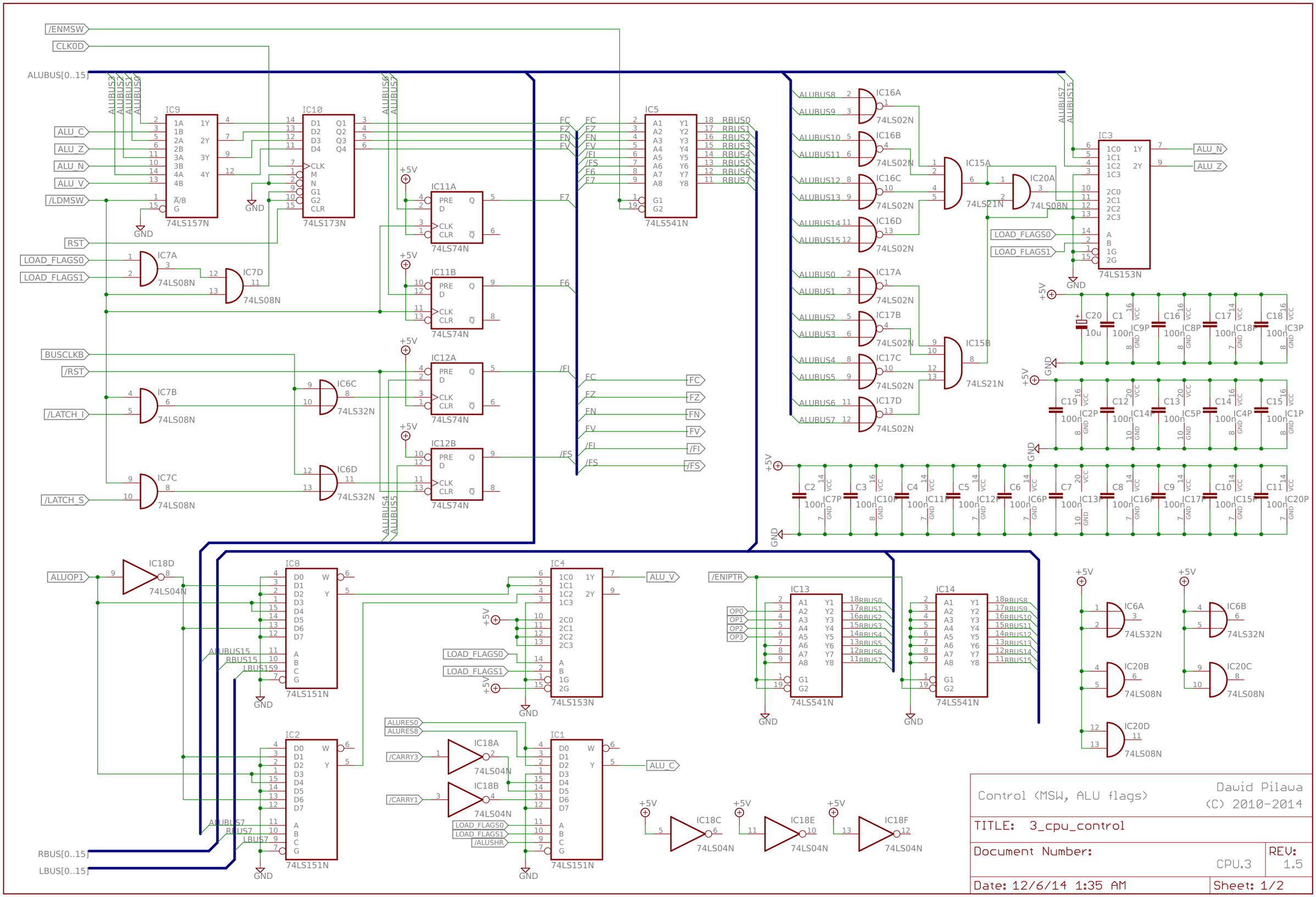


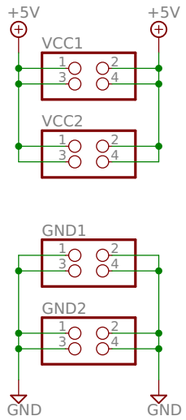



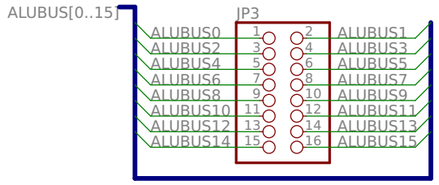



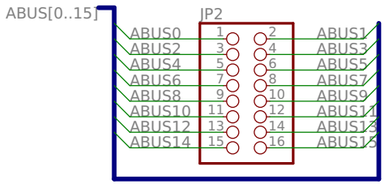

| | |
|---|---|
| Control (uROM, field decoders) | Dawid Pilawa (C) 2010-2014 |
| TITLE: 2_cpu_control | |
| Document Number: CPU.2 | REV: 1.5 |
| Date: 12/6/14 1:34 AM | Sheet: 2/2 |

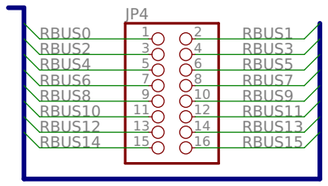

/ENMSW
CLK0D
ALUBUS[0..15]
IC9
74LS157N
IC10
74LS173N
IC5
74LS541N
ALU_C
ALU_Z
ALU_N
ALU_V
/LDMSW
RST
LOAD_FLAGS0
LOAD_FLAGS1
IC7A
IC7D
74LS08N
IC11A
IC11B
74LS74N
BUSCLKB
/RST
/LATCH_I
/LATCH_S
IC7B
IC7C
IC6C
IC6D
74LS32N
IC12A
IC12B
FC
FZ
FN
FV
/FI
/FS
F7
F6
RBUS0
RBUS1
RBUS2
RBUS3
RBUS4
RBUS5
RBUS6
RBUS7
IC16A
IC16B
IC16C
IC16D
74LS02N
IC15A
IC15B
74LS21N
IC20A
74LS08N
IC3
74LS153N
LOAD_FLAGS0
LOAD_FLAGS1
IC17A
IC17B
IC17C
IC17D
C20
10u
C1
C16
C17
C18
C19
C12
C13
C14
C15
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
100n
ALUOP1
IC18D
74LS04N
IC8
74LS151N
IC4
74LS153N
IC2
IC1
74LS151N
ALURES0
ALURES8
/CARRY3
/CARRY1
IC18A
IC18B
/ALUSHR
IC18C
IC18E
IC18F
/ENIPTR
OP0
OP1
OP2
OP3
IC13
IC14
74LS541N
IC6A
IC6B
IC20B
IC20C
IC20D
RBUS[0..15]
LBUS[0..15]
GND
+5V
Control (MSW, ALU flags)
Dawid Pilawa
(C) 2010-2014
TITLE: 3_cpu_control
Document Number:
CPU.3
REV: 1.5
Date: 12/6/14 1:35 AM
Sheet: 1/2

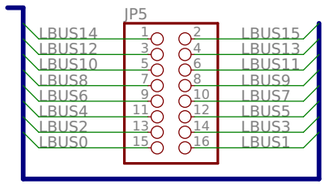
# BOARD CONNECTORS

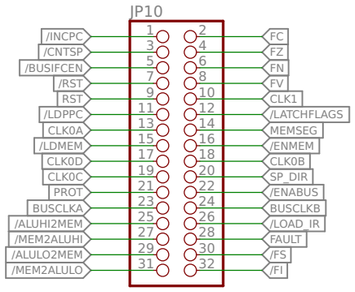


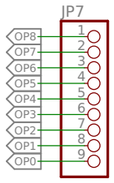



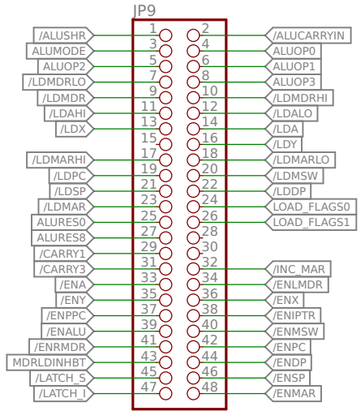



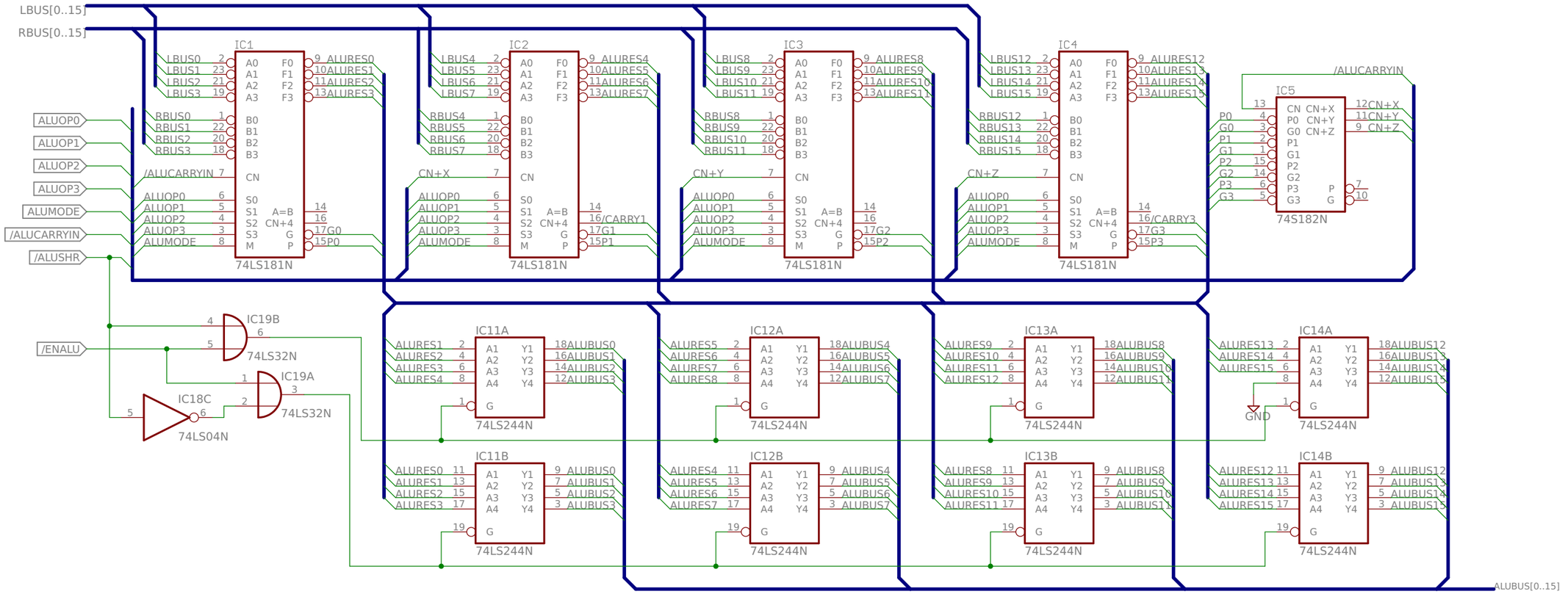



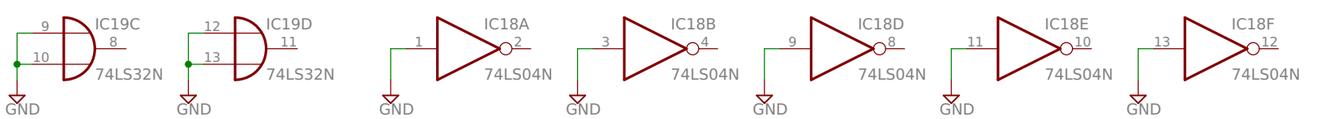



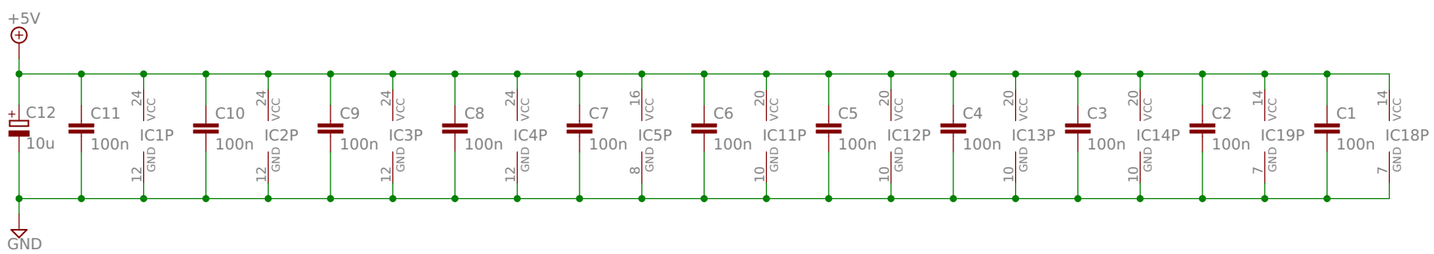




| | |
|---|---|
| Control (MSW, ALU flags) | Dawid Pilawa<br>(C) 2010-2014 |
| TITLE: 3_cpu_control | |
| Document Number: CPU.3 | REV: 1.5 |
| Date: 12/6/14 1:35 AM | Sheet: 2/2 |

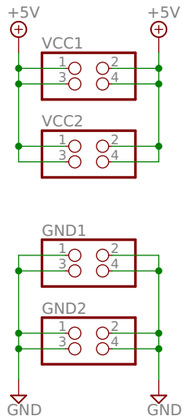


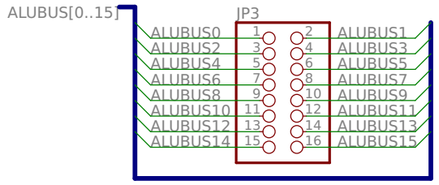



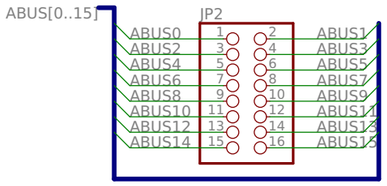



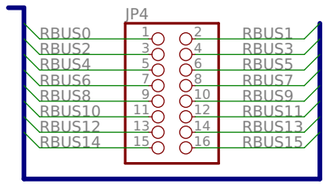

| | | |
|---|---|---|
| Arithmetic Logic Unit (ALU) | | Dawid Pilawa<br>(C) 2010-2014 |
| TITLE: 4_cpu_alu | | |
| Document Number: CPU.4 | | REV: 1.5 |
| Date: 12/6/14 1:35 AM | Sheet: 1/2 | |

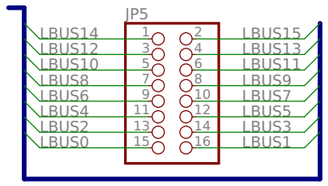
# BOARD CONNECTORS

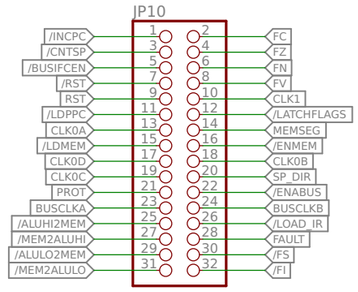


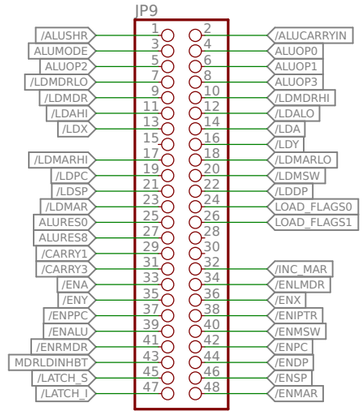



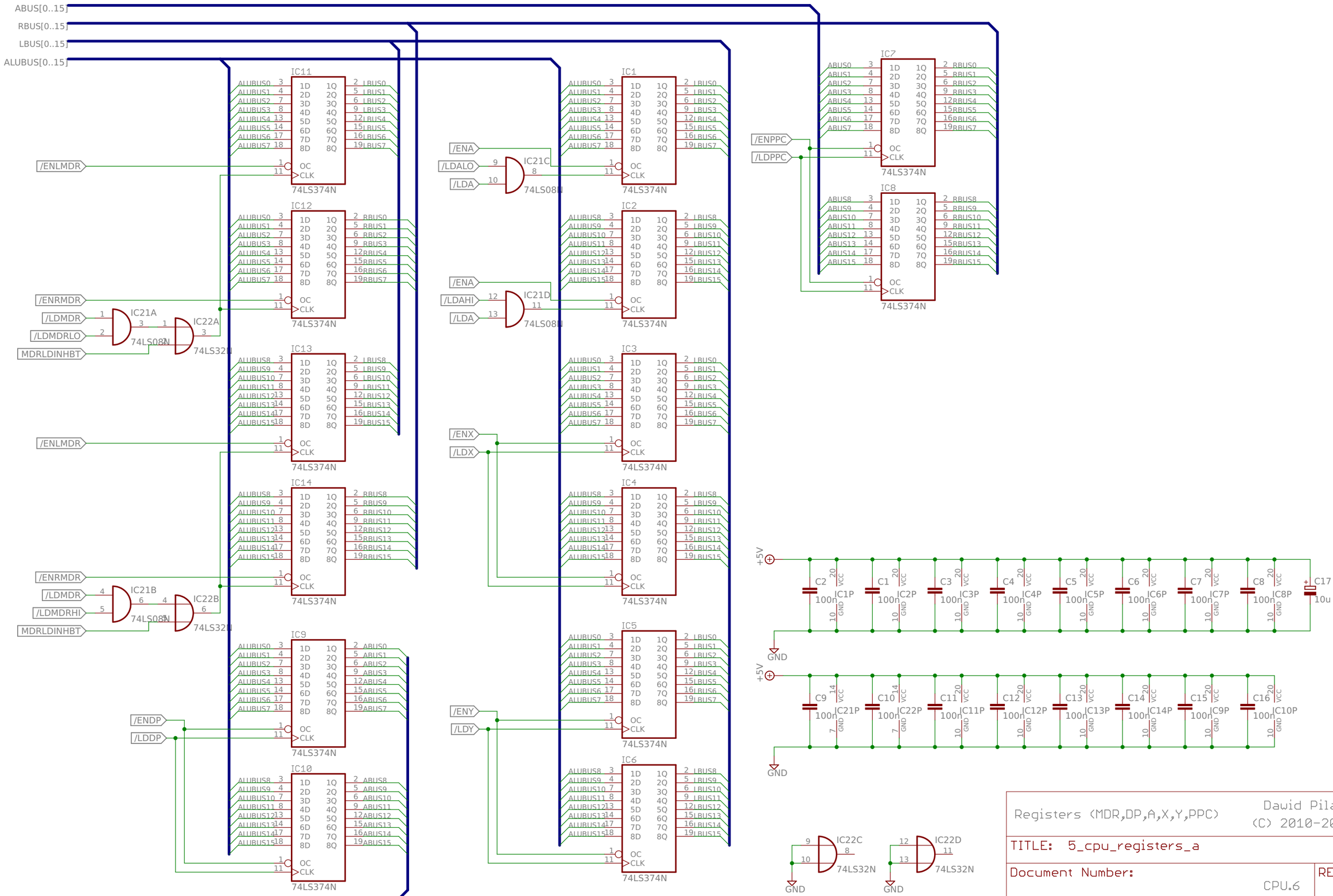



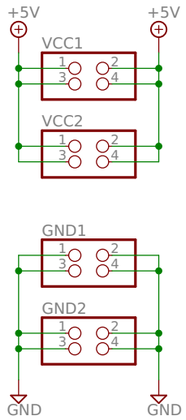



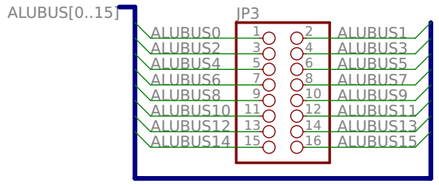



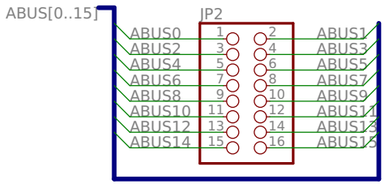

| | |
|---|---|
| Arithmetic Logic Unit (ALU) | Dawid Pilawa<br>(C) 2010-2014 |
| TITLE: 4_cpu_alu | |
| Document Number: CPU.4 | REV: 1.5 |
| Date: 12/6/14 1:35 AM | Sheet: 2/2 |

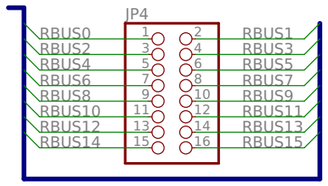

ABUS[0..15]
RBUS[0..15]
LBUS[0..15]
ALUBUS[0..15]
IC11
IC12
IC13
IC14
IC9
IC10
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
74LS374N
/ENLMDR
/ENRMDR
/LDMDR
/LDMDRLO
/LDMDRHI
MDRLDINHBT
IC21A
IC22A
IC21B
IC22B
74LS08N
74LS32N
/ENA
/LDALO
/LDA
/LDAHI
IC21C
IC21D
/ENX
/LDX
/ENY
/LDY
/ENPPC
/LDPPC
/ENDP
/LDDP
IC22C
IC22D
+5V
GND
C1
C2
C3
C4
C5
C6
C7
C8
C17
C9
C10
C11
C12
C13
C14
C15
C16
100n
10u
IC1P
IC2P
IC3P
IC4P
IC5P
IC6P
IC7P
IC8P
IC9P
IC10P
IC11P
IC12P
IC13P
IC14P
IC21P
IC22P
Registers (MDR,DP,A,X,Y,PPC)
Dawid Pilawa
(C) 2010-2014
TITLE: 5_cpu_registers_a
Document Number:
CPU.6
REV:
1.5
Date: 12/6/14 1:35 AM
Sheet: 1/2

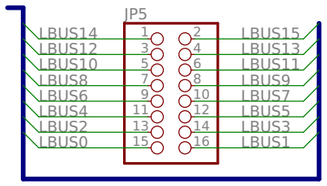
# BOARD CONNECTORS

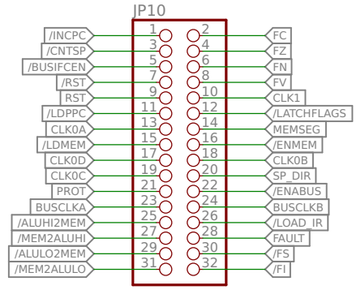


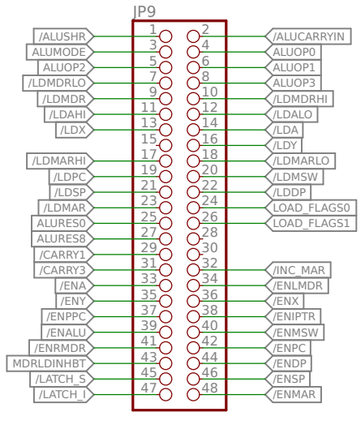




| | |
|---|---|
| Registers (MDR,DP,A,X,Y,PPC) | Dawid Pilawa<br>(C) 2010-2014 |
| TITLE: 5_cpu_registers_a | |
| Document Number: CPU.6 | REV: 1.5 |
| Date: 12/6/14 1:35 AM | Sheet: 2/2 |

/INC_MAR
/ENMAR
/LDMAR
/LDMARLO
/LDMARHI
CLK0B
/RST
ABUS[0..15]
ALUBUS[0..15]
/INCPC
/LDPC
/ENPC
/CNTSP
/LDSP
SP_DIR
/ENSP
/FS
CLK0C

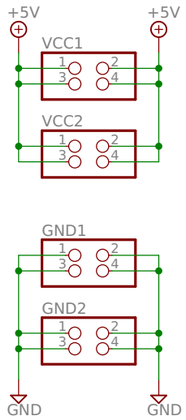
+5V
GND
C19 100n
C20 10u
IC9P
IC9C
IC9D
74LS08N

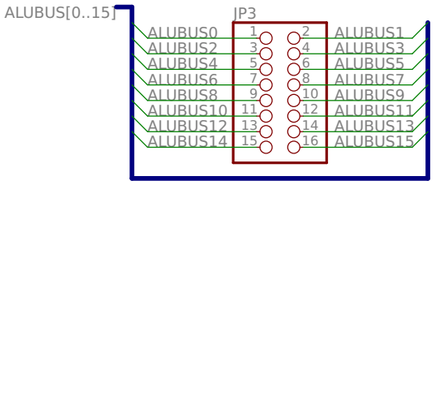
IC1 IC2 IC3 IC4 IC5 IC6 IC7 IC8 IC12 IC13 IC14 IC15 IC16 IC17 IC18 IC19
74LS569
IC10 IC11
74LS157N
IC9A IC9B
74LS08N

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18
100n

| | |
|---|---|
| Registers (MAR,PC,KSP,SP) | Dawid Pilawa (C) 2010-2014 |
| TITLE: 6_cpu_registers_b | |
| Document Number: CPU.5 | REV: 1.5 |
| Date: 12/6/14 1:36 AM | Sheet: 1/2 |

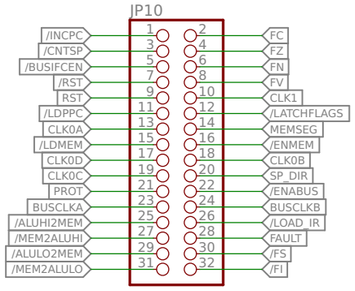
# BOARD CONNECTORS

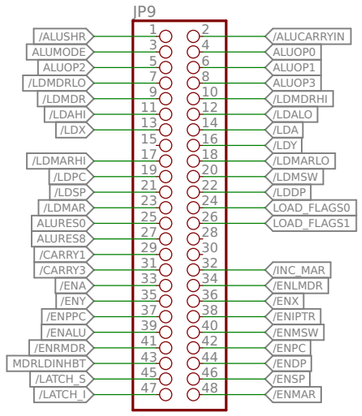









| | |
|---|---|
| Registers (MAR,PC,KSP,SP) | Dawid Pilawa<br>(C) 2010-2014 |
| TITLE: 6_cpu_registers_b | |
| Document Number: CPU.5 | REV: 1.5 |
| Date: 12/6/14 1:36 AM | Sheet: 2/2 |

+5V
GND
C20 10uF
C1 100n
C2 100n
C3 100n
C4 100n
C5 100n
C6 100n
C7 100n
C8 100n
C9 100n
IC1P IC2P IC3P IC4P IC5P IC6P IC7P IC8P IC9P
C10 100n
C11 100n
C12 100n
C13 100n
C14 100n
C15 100n
C16 100n
C17 100n
C18 100n
C19 100n
IC10P IC11P IC12P IC13P IC14P IC17P IC18P IC19P
VCC GND

IC1 IC2 IC3 IC4
74LS374N
IDBUS0 IDBUS1 IDBUS2 IDBUS3 IDBUS4 IDBUS5 IDBUS6 IDBUS7
PBUS15 PBUS16 PBUS17 PBUS18 PBUS19 PBUS20 PBUS21
/ENUCODE0 /LDUCODE0
/ENUCODE1 /LDUCODE1
/ENUDATA0 /LDUDATA0
/ENUDATA1 /LDUDATA1
OC CLK

IC5 IC11
74LS138N
ABUS15 MEMSEG /FS
ABUS9 ABUS10 ABUS11
G1 G2A G2B
A B C
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
/ENSCODE0 /ENSCODE1 /ENSDATA0 /ENSDATA1 /ENUCODE0 /ENUCODE1 /ENUDATA0 /ENUDATA1
/LDSCODE0 /LDSCODE1 /LDSDATA0 /LDSDATA1 /LDUCODE0 /LDUCODE1 /LDUDATA0 /LDUDATA1

IC6 IC7 IC8 IC9 IC10
74LS273N
74LS541N
74LS374N
D1 D2 D3 D4 D5 D6 D7 D8
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
CLK CLR
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2

J1
DIN41612
DBUS0 DBUS1 DBUS2 DBUS3 DBUS4 DBUS5 DBUS6 DBUS7 /IO
/RST MEMSEG /I DMEM /ENMEM
ABUS1 ABUS3 ABUS5 ABUS7 ABUS9 ABUS11 ABUS13 ABUS15
ABUS0 ABUS2 ABUS4 ABUS6 ABUS8 ABUS10 ABUS12 ABUS14

IC12
74LS245N
DIR G
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
RN1 4k7

IC13A IC13B IC13C IC13D IC13E IC13F
74LS04N
IC17A IC17B IC17C IC17D
74LS32N

IC14NC2
IC14
AM29F010
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
O0 O1 O2 O3 O4 O5 O6 O7
CE OE WE/

IC15 IC16
628512
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
I/O00 I/O01 I/O02 I/O03 I/O04 I/O05 I/O06 I/O07
VCC VSS CE WE OE

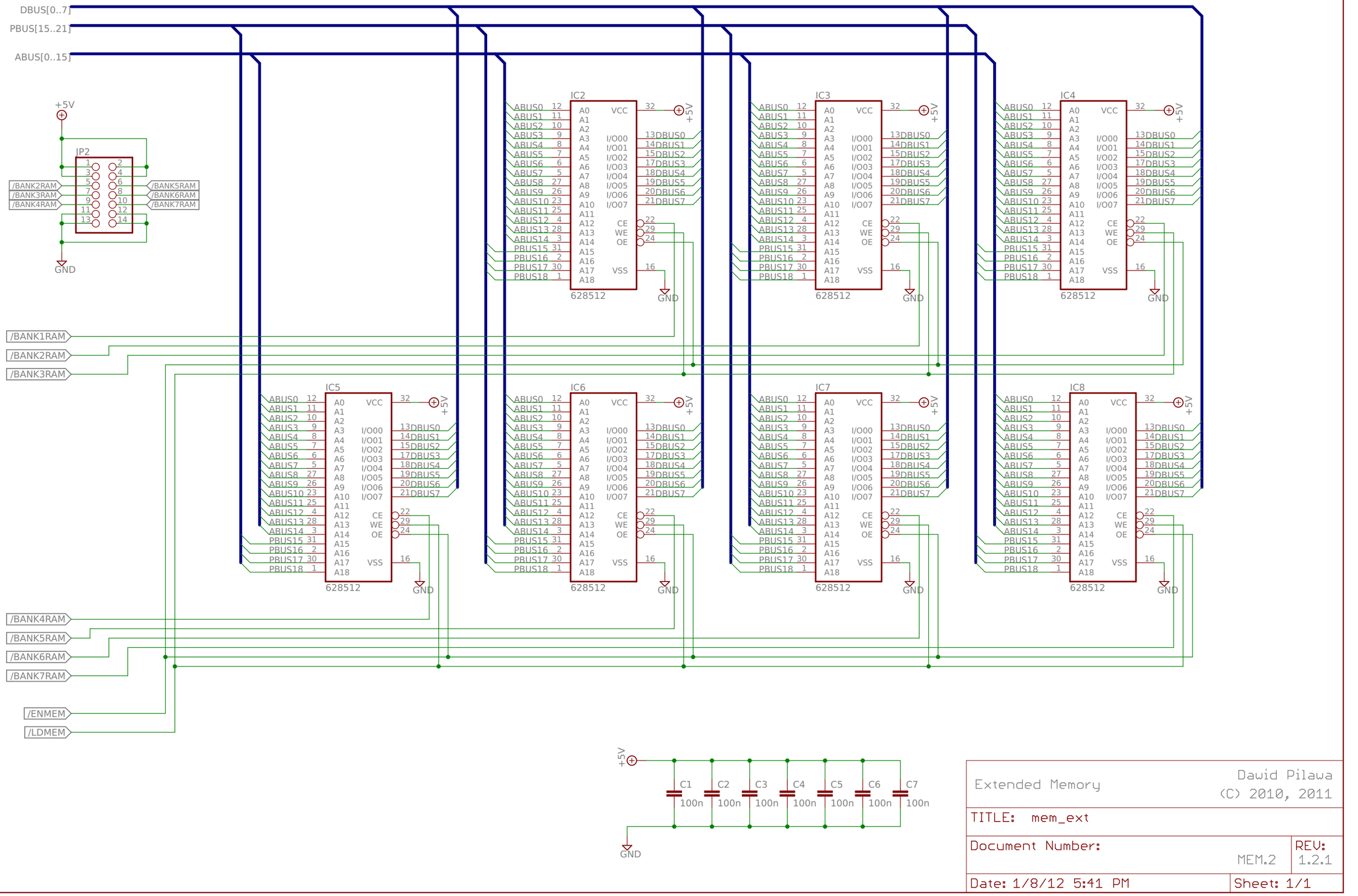
IC18
74LS138N
/BANK2RAM /BANK3RAM /BANK4RAM /BANK5RAM /BANK6RAM /BANK7RAM

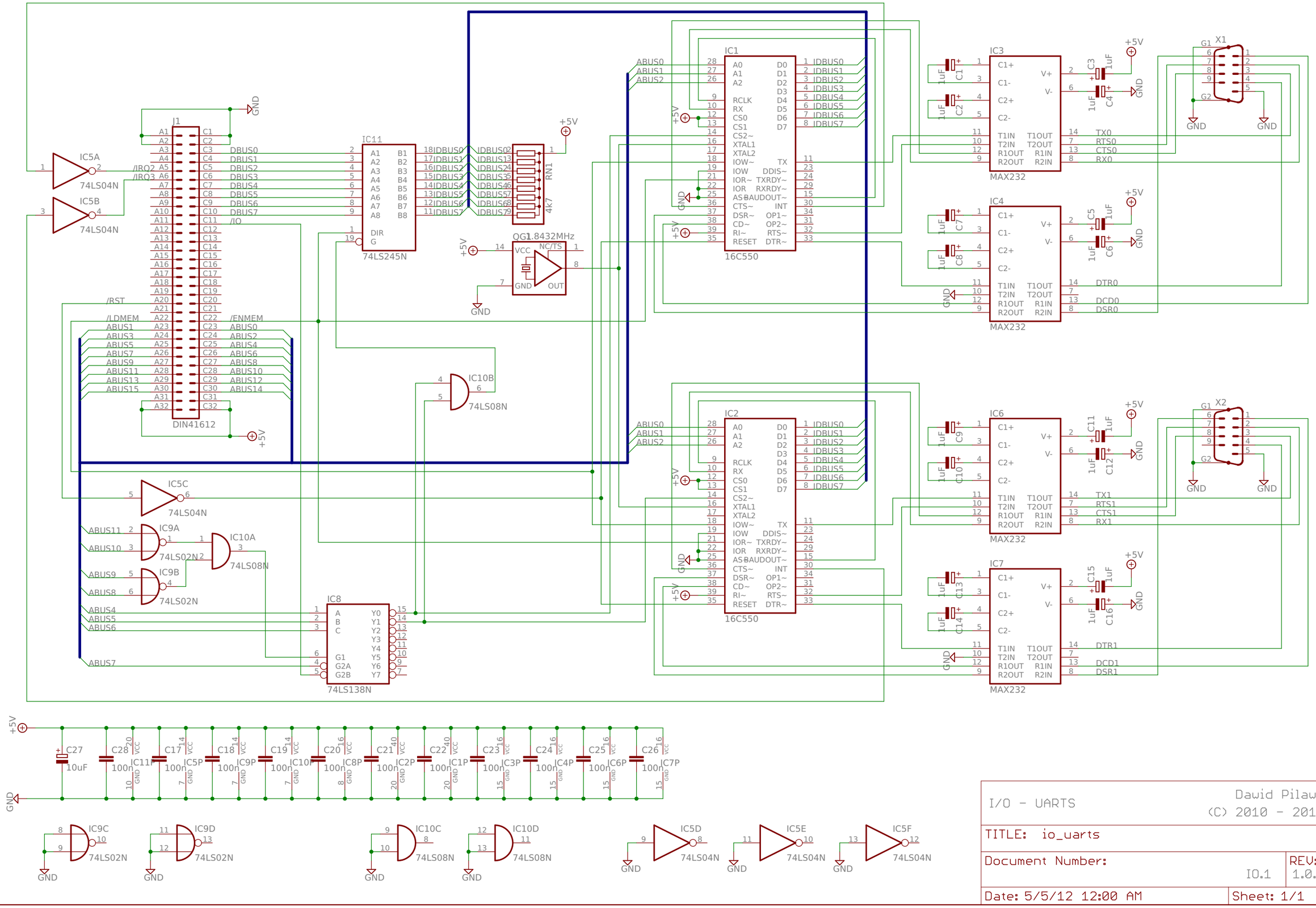
IC19
74LS138N

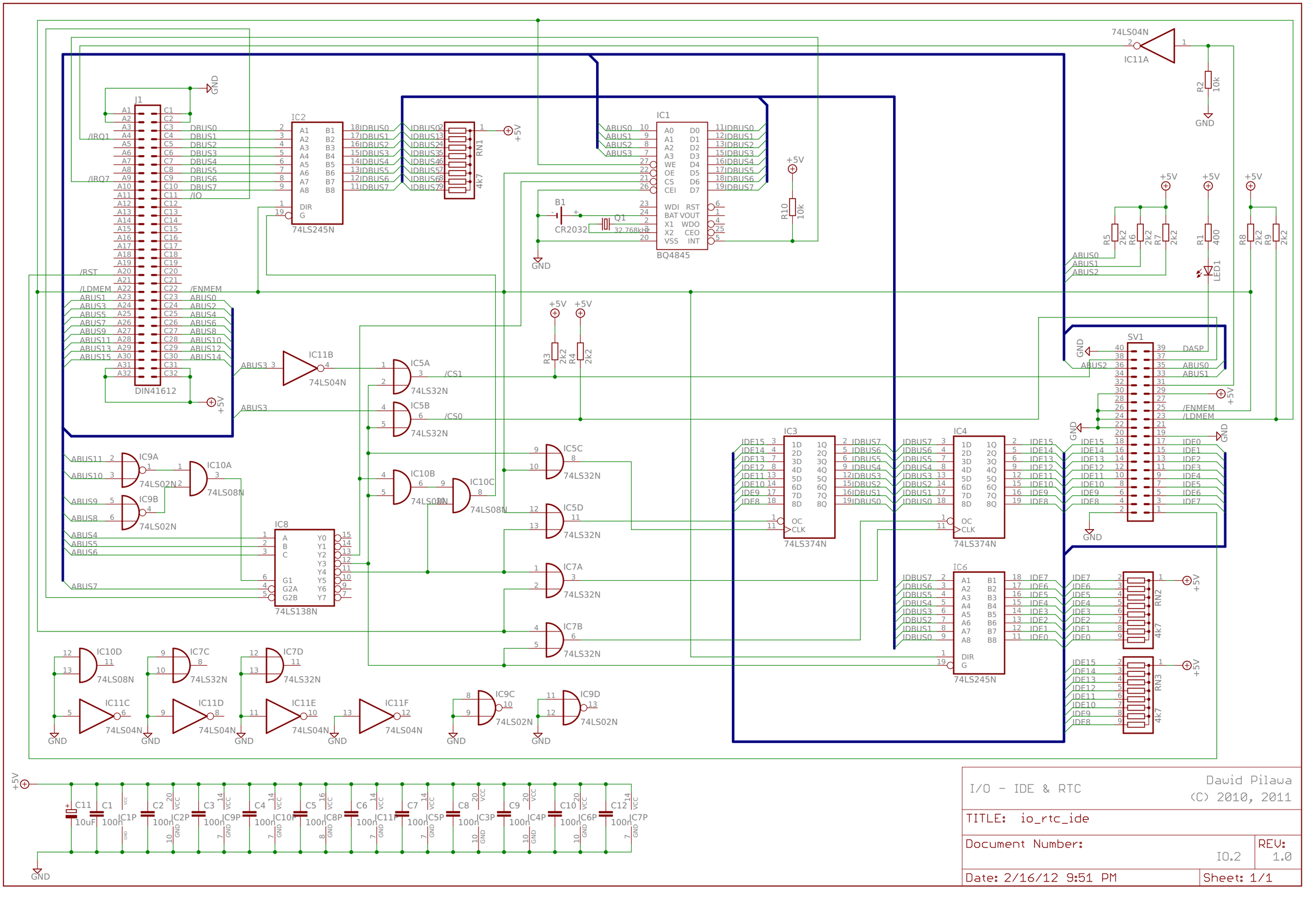
JP1

Dawid Pilawa
Base Memory - address decoder (C) 2010, 2011

| | |
|---|---|
| TITLE: mem_base | |
| Document Number: MEM.1 | REV: 1.2.1 |
| Date: 11/6/11 8:26 PM | Sheet: 1/1 |


DBUS[0..7]
PBUS[15..21]
ABUS[0..15]
+5V
JP2
/BANK2RAM
/BANK3RAM
/BANK4RAM
/BANK5RAM
/BANK6RAM
/BANK7RAM
GND
IC2
IC3
IC4
IC5
IC6
IC7
IC8
628512
/BANK1RAM
/BANK2RAM
/BANK3RAM
/BANK4RAM
/BANK5RAM
/BANK6RAM
/BANK7RAM
/ENMEM
/LDMEM
C1
C2
C3
C4
C5
C6
C7
100n
Extended Memory
Dawid Pilawa
(C) 2010, 2011
TITLE: mem_ext
Document Number:
MEM.2
REV:
1.2.1
Date: 1/8/12 5:41 PM
Sheet: 1/1


J1
DIN41612
IC11
74LS245N
IC1
16C550
IC2
16C550
IC3
MAX232
IC4
MAX232
IC6
MAX232
IC7
MAX232
IC8
74LS138N
RN1
4k7
QG1 8.432MHz
X1
X2
IC5A
74LS04N
IC5B
74LS04N
IC5C
74LS04N
IC9A
74LS02N
IC9B
74LS02N
IC10A
74LS08N
IC10B
74LS08N
IC9C
74LS02N
IC9D
74LS02N
IC10C
74LS08N
IC10D
74LS08N
IC5D
74LS04N
IC5E
74LS04N
IC5F
74LS04N
/IRQ2
/IRQ3
/RST
/LDMEM
/ENMEM
/IO
DBUS0
DBUS1
DBUS2
DBUS3
DBUS4
DBUS5
DBUS6
DBUS7
ABUS0
ABUS1
ABUS2
ABUS4
ABUS5
ABUS6
ABUS7
ABUS8
ABUS9
ABUS10
ABUS11
ABUS12
ABUS13
ABUS14
ABUS15
IDBUS0
IDBUS1
IDBUS2
IDBUS3
IDBUS4
IDBUS5
IDBUS6
IDBUS7
TX0
RTS0
CTS0
RX0
DTR0
DCD0
DSR0
TX1
RTS1
CTS1
RX1
DTR1
DCD1
DSR1
+5V
GND
C27 10uF
C28 100n
C17 100n
C18 100n
C19 100n
C20 100n
C21 100n
C22 100n
C23 100n
C24 100n
C25 100n
C26 100n
I/O - UARTS
Dawid Pilawa
(C) 2010 - 2012
TITLE: io_uarts
Document Number: IO.1
REV: 1.0.3
Date: 5/5/12 12:00 AM
Sheet: 1/1







| | |
|---|---|
| I/O - IDE & RTC | Dawid Pilawa<br>(C) 2010, 2011 |
| TITLE: io_rtc_ide | |
| Document Number: IO.2 | REV: 1.0 |
| Date: 2/16/12 9:51 PM | Sheet: 1/1 |