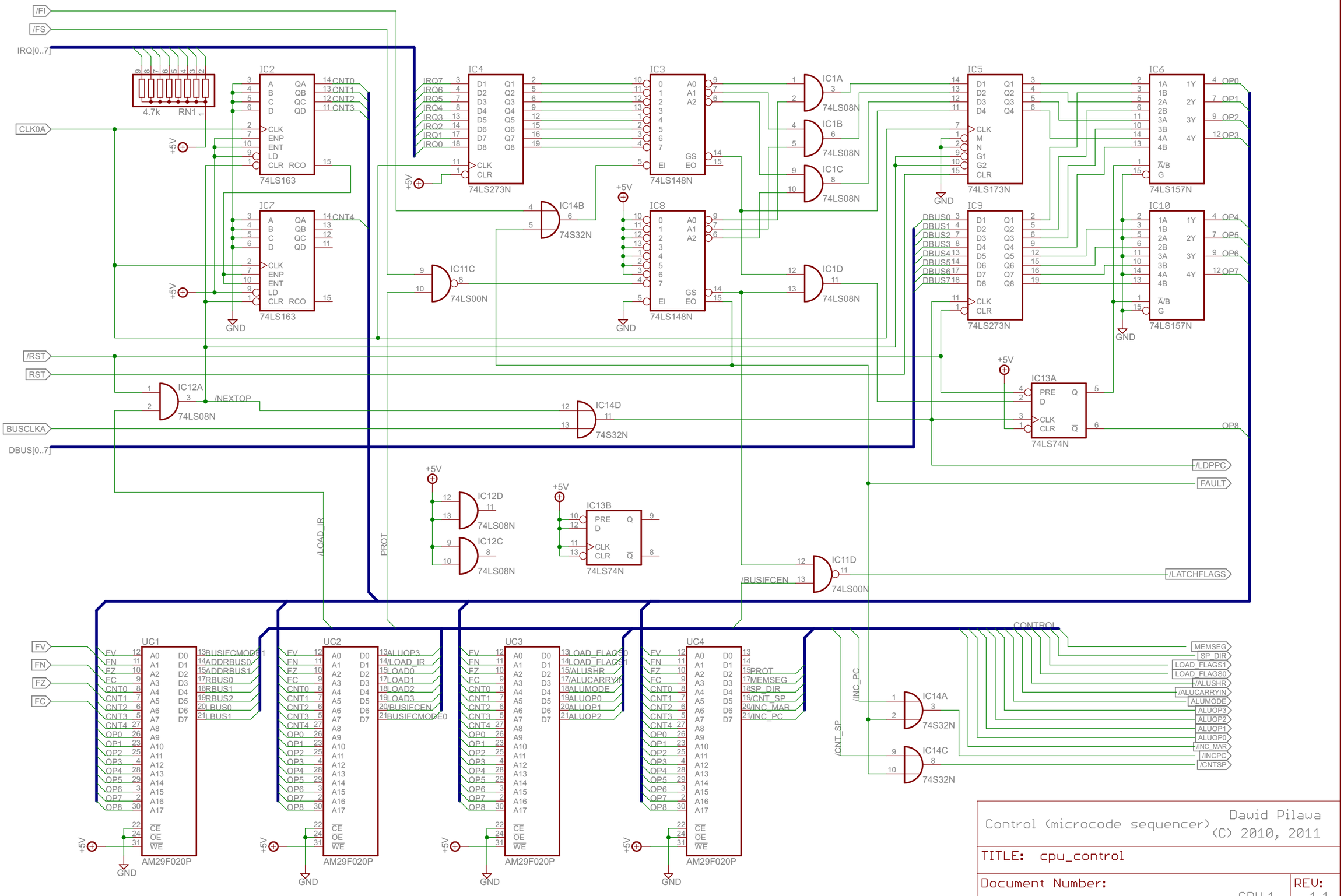


Control (microcode sequencer)

Dawid Pilawa
(C) 2010, 2011

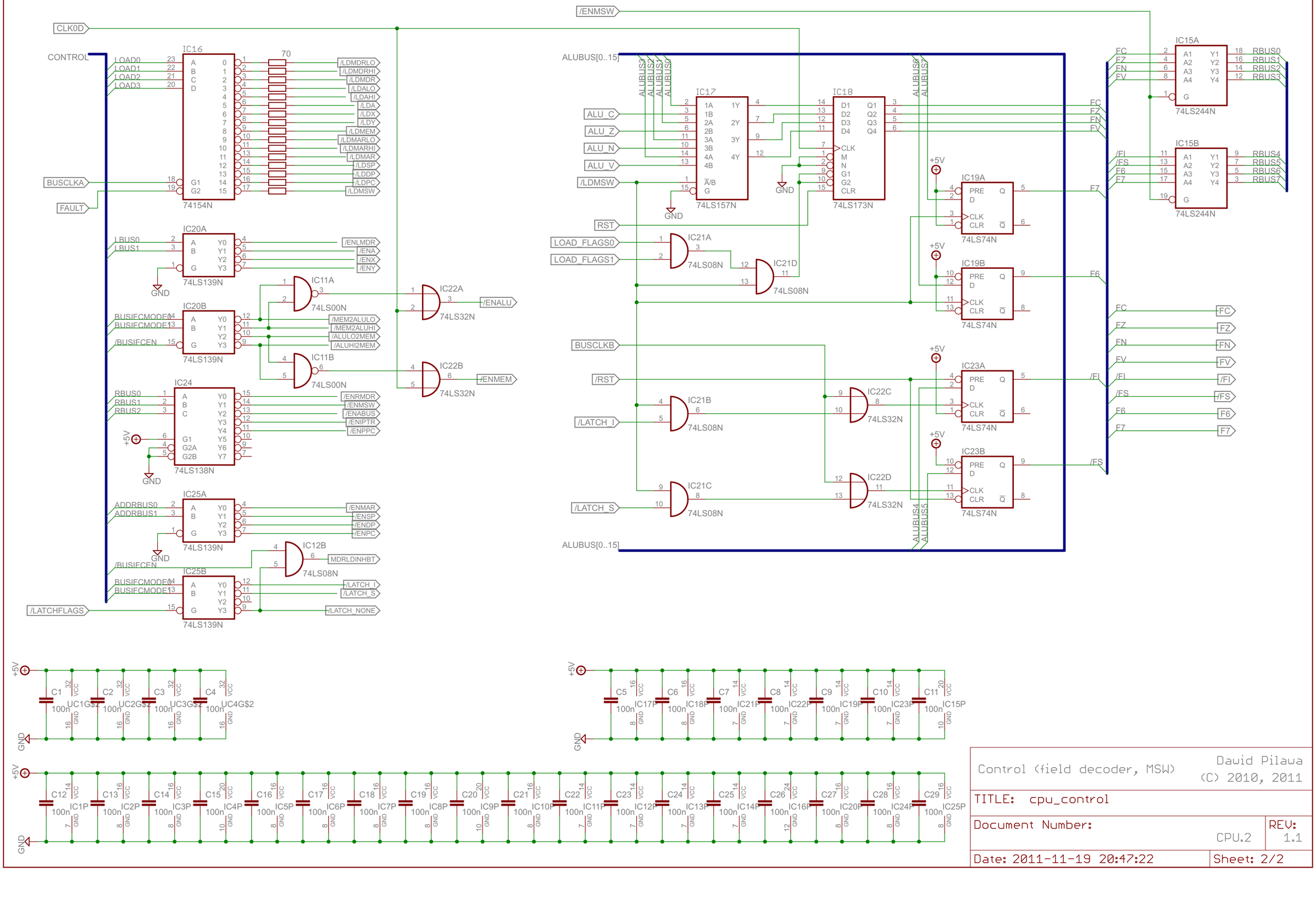
TITLE: cpu_control

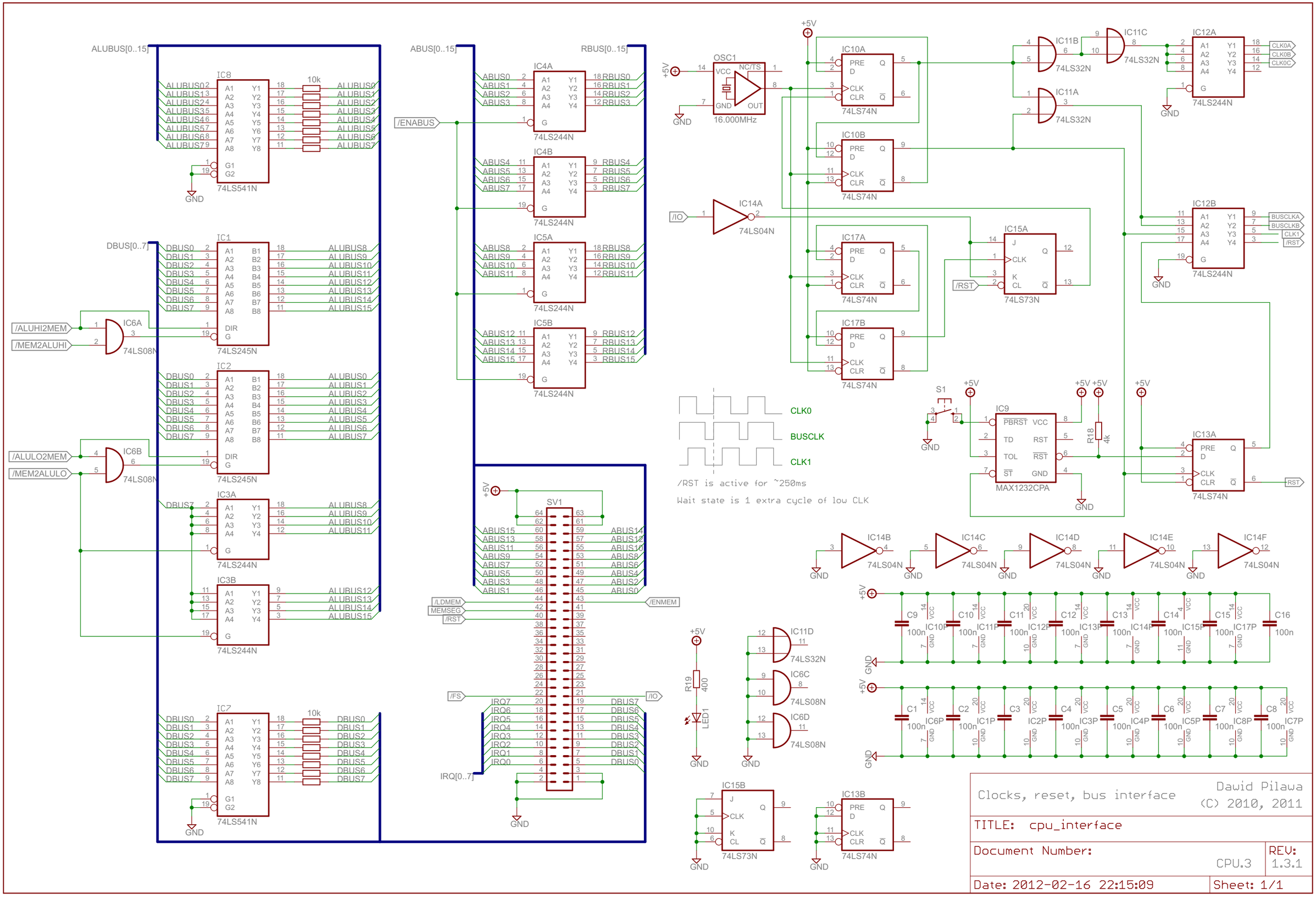
Document Number: CPU.1

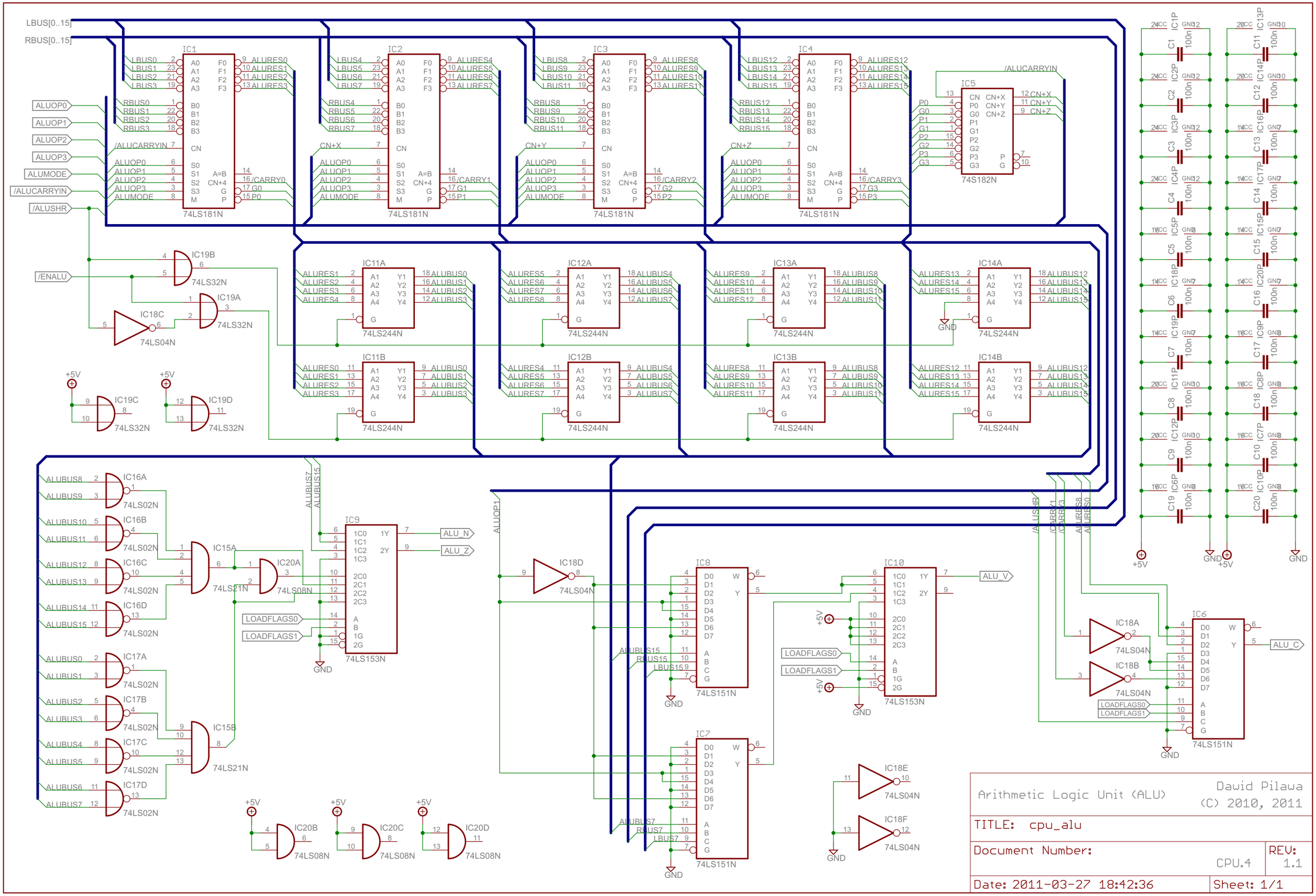
REV: 1.1

Date: 2011-11-19 20:47:22

Sheet: 1/2


CLK0D
/ENMSW
CONTROL
ALUBUS[0..15]
IC16
74154N
70
/LDMDRLO
/LDMDRHI
/LDMDR
/LDALO
/LDAHI
/LDA
/LDX
/LDY
/LDMEM
/LDMARLO
/LDMARHI
/LDMAR
/LDSP
/LDDP
/LDPC
/LDMSW
BUSCLKA
FAULT
IC17
74LS157N
IC18
74LS173N
ALU_C
ALU_Z
ALU_N
ALU_V
/LDMSW
GND
RST
LOAD_FLAGS0
LOAD_FLAGS1
IC21A
74LS08N
IC21D
74LS08N
IC19A
74LS74N
IC19B
74LS74N
+5V
IC15A
74LS244N
IC15B
74LS244N
FC
FZ
FN
FV
/FI
/FS
F6
F7
RBUS0
RBUS1
RBUS2
RBUS3
RBUS4
RBUS5
RBUS6
RBUS7
IC20A
74LS139N
/ENLMDR
/ENA
/ENX
/ENY
IC11A
74LS00N
IC22A
74LS32N
/ENALU
IC20B
74LS139N
/MEM2ALULO
/MEM2ALUHI
/ALULO2MEM
/ALUHI2MEM
IC11B
74LS00N
IC22B
74LS32N
/ENMEM
BUSIFCMODE0
BUSIFCMODE1
/BUSIFCEN
BUSCLKB
/RST
/LATCH_I
IC24
74LS138N
/ENRMDR
/ENMSW
/ENABUS
/ENIPTR
/ENPPC
IC21B
74LS08N
IC22C
74LS32N
IC23A
74LS74N
IC23B
74LS74N
IC21C
74LS08N
IC22D
74LS32N
/LATCH_S
ALUBUS4
ALUBUS5
IC25A
74LS139N
/ENMAR
/ENSP
/ENDP
/ENPC
IC12B
74LS08N
MDRLDINHBT
IC25B
74LS139N
/LATCH_I
/LATCH_S
/LATCH_NONE
/LATCHFLAGS
C1
C2
C3
C4
100n
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
Control (field decoder, MSW)
Dawid Pilawa
(C) 2010, 2011
TITLE: cpu_control
Document Number:
CPU.2
REV:
1.1
Date: 2011-11-19 20:47:22
Sheet: 2/2


ALUBUS[0..15]
IC8
10k
74LS541N
GND
DBUS[0..7]
IC1
74LS245N
/ALUHI2MEM
/MEM2ALUHI
IC6A
74LS08N
IC2
/ALULO2MEM
/MEM2ALULO
IC6B
IC3A
74LS244N
IC3B
IC7
ABUS[0..15]
RBUS[0..15]
IC4A
IC4B
IC5A
IC5B
/ENABUS
SV1
/LDMEM
MEMSEG
/RST
/FS
/IO
/ENMEM
IRQ[0..7]
+5V
OSC1
16.000MHz
IC10A
IC10B
74LS74N
IC14A
74LS04N
IC17A
IC17B
IC11B
IC11C
IC11A
74LS32N
IC12A
IC12B
74LS244N
IC15A
74LS73N
CLK0
BUSCLK
CLK1
/RST is active for ~250ms
Wait state is 1 extra cycle of low CLK
S1
IC9
MAX1232CPA
R18
4k
IC13A
IC13B
74LS74N
IC11D
IC6C
IC6D
74LS08N
R19
400
LED1
IC15B
IC14B
IC14C
IC14D
IC14E
IC14F
74LS04N
C9
C10
C11
C12
C13
C14
C15
C16
C1
C2
C3
C4
C5
C6
C7
C8
100n
Clocks, reset, bus interface
Dawid Pilawa
(C) 2010, 2011
TITLE: cpu_interface
Document Number:
CPU.3
REV:
1.3.1
Date: 2012-02-16 22:15:09
Sheet: 1/1



Arithmetic Logic Unit (ALU)

Dawid Pilawa
(C) 2010, 2011

TITLE: cpu_alu

Document Number: CPU.4

REV: 1.1

Date: 2011-03-27 18:42:36

Sheet: 1/1

/INC_MAR
/ENMAR
/LDMAR
/LDMARLO
/LDMARHI
CLK0B
/RST
ABUS[0..15]
ALUBUS[0..15]
/INCPC
/LDPC
/ENPC
/CNTSP
/LDSP
SP_DIR
/ENSP
/FS
CLK0C

IC1 IC2 IC3 IC4 IC5 IC6 IC7 IC8 IC12 IC13 IC14 IC15 IC16 IC17 IC18 IC19
74LS569
IC9A IC9B
74LS08N
IC9C IC9D
74LS08N
IC10 IC11
74LS157N
C19 IC9P
100n
+5V
GND

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18
100n
IC1P IC2P IC3P IC4P IC5P IC6P IC7P IC8P IC10P IC12P IC13P IC14P IC11P IC16P IC17P IC18P IC19P

Registers (MAR,PC,KSP,SP)	Dawid Pilawa (C) 2010, 2011
TITLE: cpu_registers1	
Document Number: CPU.5	REV: 1.1
Date: 2011-03-27 18:46:14	Sheet: 1/1

ABUS[0..15]
RBUS[0..15]
LBUS[0..15]
ALUBUS[0..15]

/ENMDRL
/ENMDRR
/LDMDR
/LDMDRLO
MDRLDINHBT
/LDMDRHI
/ENDP
/LDDP
/ENA
/LDALO
/LDA
/LDAHI
/ENX
/LDX
/ENY
/LDY
/ENIPTR
OP0
OP1
OP2
OP3
/ENPPC
/LDPPC

IC11, IC12, IC13, IC14, IC9, IC10, IC1, IC2, IC3, IC4, IC5, IC6, IC7, IC8 — 74LS374N
IC21A, IC21B, IC21C, IC21D — 74LS08N
IC22A, IC22B — 74LS32N
IC19A, IC19B, IC20A, IC20B — 74LS244N
GND
+5V
C1–C18 — 100n
IC1P, IC2P, IC3P, IC4P, IC5P, IC6P, IC7P, IC8P, IC9P, IC10P, IC11P, IC12P, IC13P, IC14P, IC19P, IC20P, IC21P, IC22P

Registers (MDR,DP,A,X,Y,PPC,IPTR)
Dawid Pilawa
(C) 2010, 2011

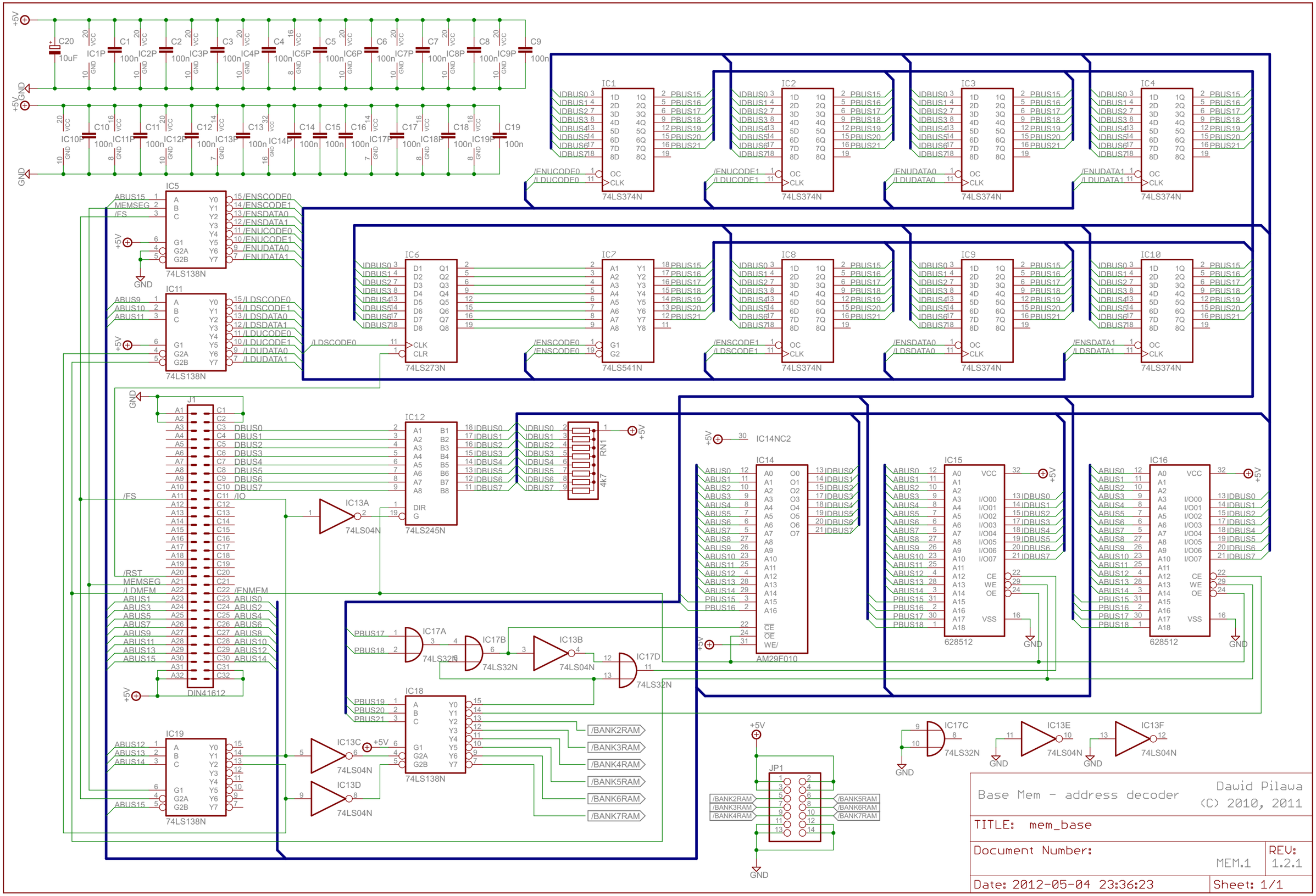
TITLE: cpu_registers2

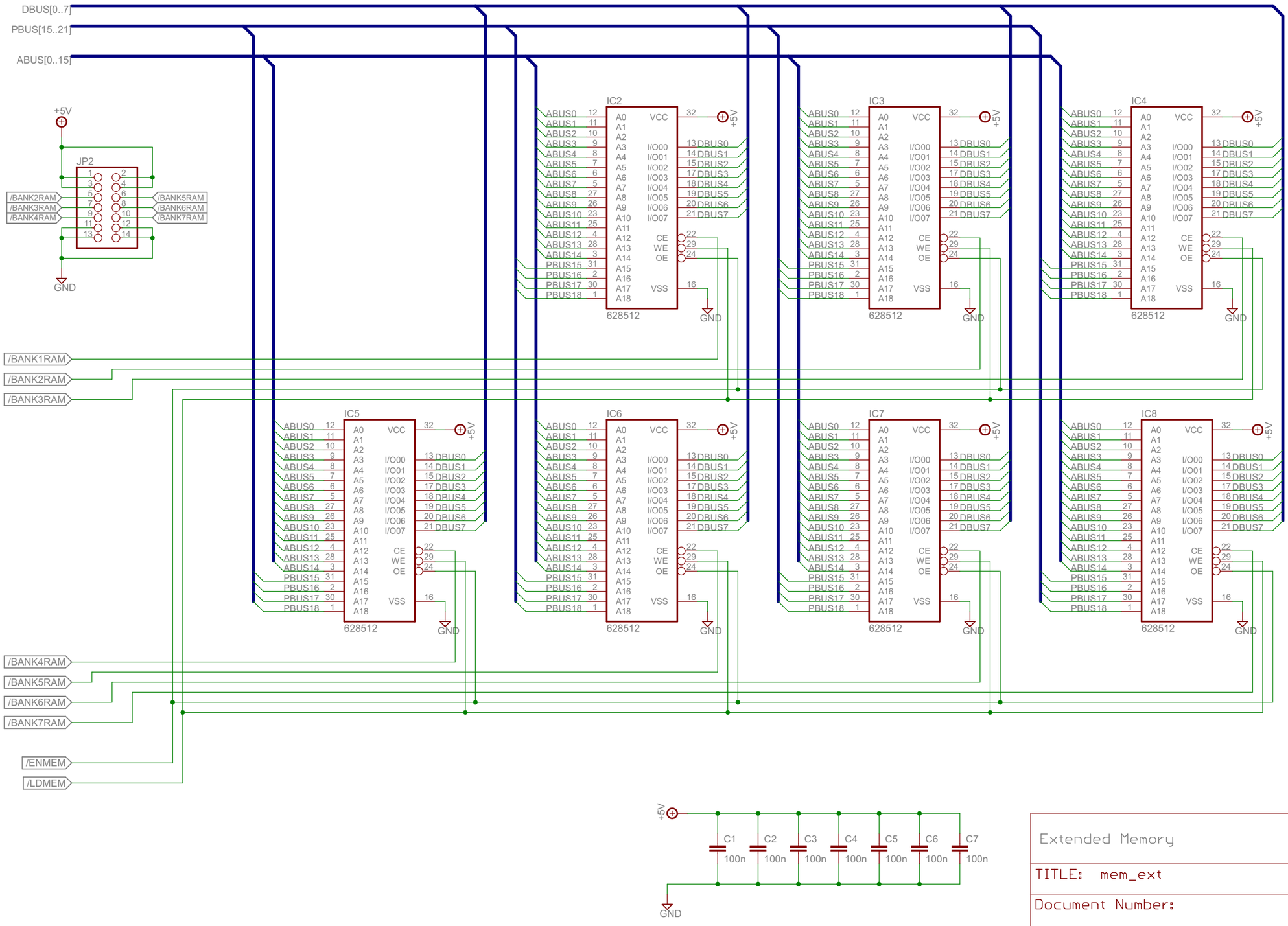
Document Number: CPU.6

REV: 1.1

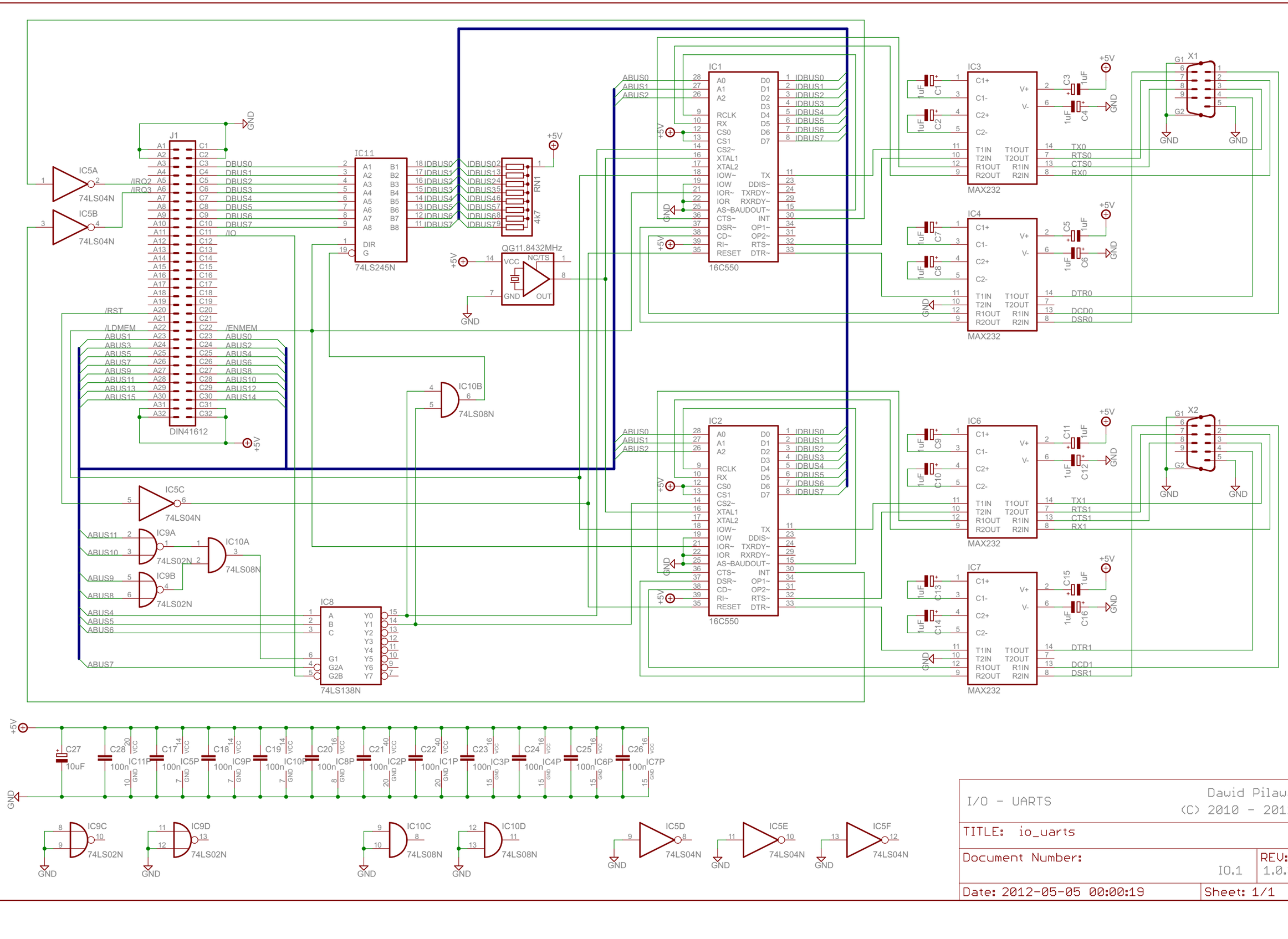
Date: 2011-03-27 18:47:12

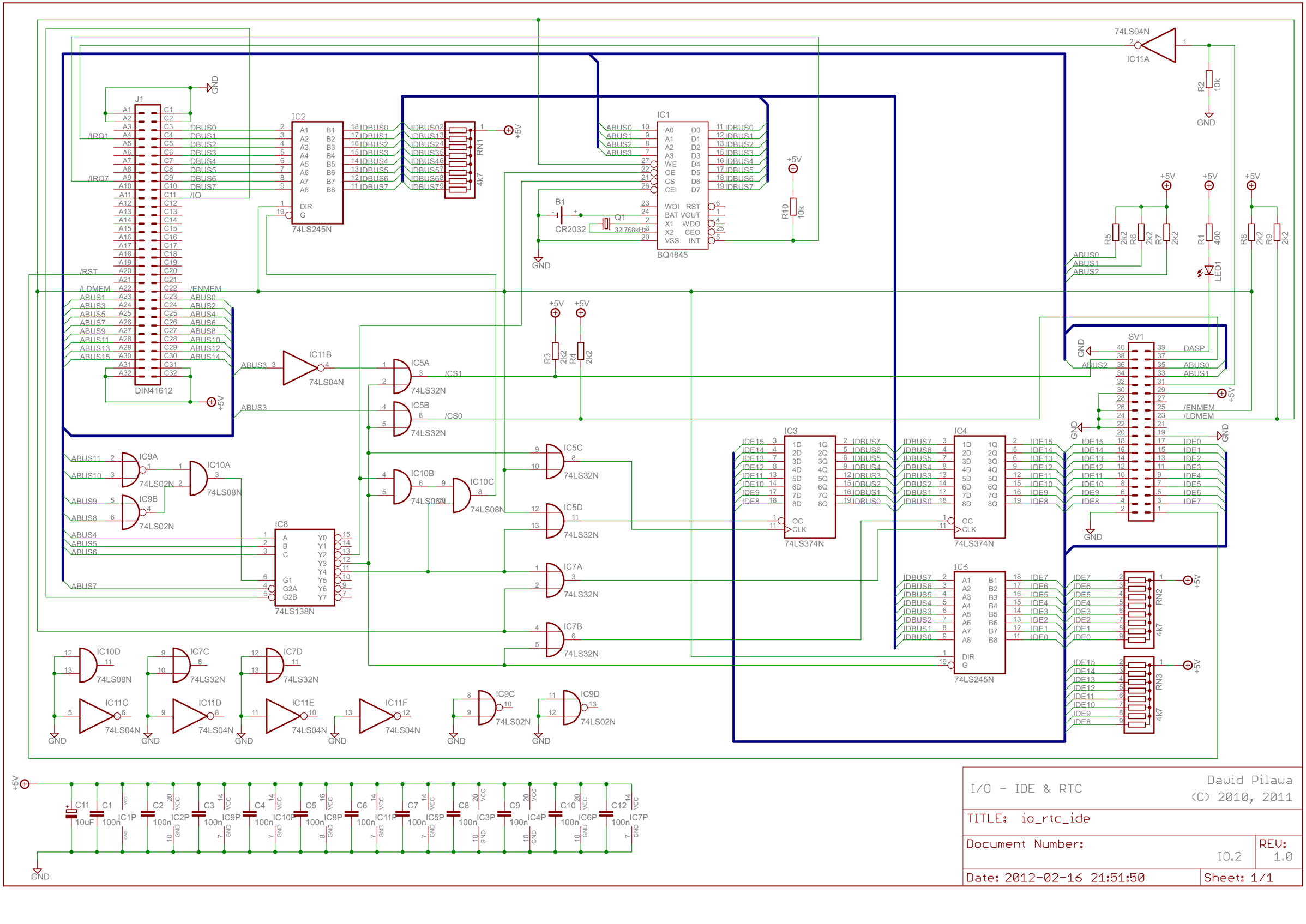
Sheet: 1/1


+5V
GND
C20 10uF
C1 100n
C2 100n
C3 100n
C4 100n
C5 100n
C6 100n
C7 100n
C8 100n
C9 100n
C10 100n
C11 100n
C12 100n
C13 100n
C14 100n
C15 100n
C16 100n
C17 100n
C18 100n
C19 100n
IC1
IC2
IC3
IC4
74LS374N
/ENUCODE0
/LDUCODE0
/ENUCODE1
/LDUCODE1
/ENUDATA0
/LDUDATA0
/ENUDATA1
/LDUDATA1
IC5
74LS138N
ABUS15
MEMSEG
/FS
/ENSCODE0
/ENSCODE1
/ENSDATA0
/ENSDATA1
/ENUCODE0
/ENUCODE1
/ENUDATA0
/ENUDATA1
IC6
74LS273N
IC7
74LS541N
IC8
IC9
IC10
IC11
ABUS9
ABUS10
ABUS11
/LDSCODE0
/LDSCODE1
/LDSDATA0
/LDSDATA1
/LDUCODE0
/LDUCODE1
/LDUDATA0
/LDUDATA1
/ENSCODE0
/ENSCODE1
/ENSDATA0
/ENSDATA1
J1
DIN41612
DBUS0
DBUS1
DBUS2
DBUS3
DBUS4
DBUS5
DBUS6
DBUS7
/IO
/RST
MEMSEG
/I DMEM
/ENMEM
IC12
74LS245N
IDBUS0
IDBUS1
IDBUS2
IDBUS3
IDBUS4
IDBUS5
IDBUS6
IDBUS7
RN1
4k7
IC13A
74LS04N
IC13B
IC13C
IC13D
IC13E
IC13F
IC14NC2
IC14
AM29F010
ABUS0
ABUS1
ABUS2
ABUS3
ABUS4
ABUS5
ABUS6
ABUS7
ABUS8
ABUS9
ABUS10
ABUS11
ABUS12
ABUS13
ABUS14
PBUS15
PBUS16
PBUS17
PBUS18
IC15
IC16
628512
IC17A
IC17B
IC17C
IC17D
74LS32N
IC18
IC19
/BANK2RAM
/BANK3RAM
/BANK4RAM
/BANK5RAM
/BANK6RAM
/BANK7RAM
JP1
Base Mem - address decoder
Dawid Pilawa
(C) 2010, 2011
TITLE: mem_base
Document Number:
MEM.1
REV:
1.2.1
Date: 2012-05-04 23:36:23
Sheet: 1/1



Extended Memory	Dawid Pilawa (C) 2010, 2011
TITLE: mem_ext	
Document Number: MEM.2	REV: 1.2.1
Date: 2012-01-08 17:41:52	Sheet: 1/1


J1
DIN41612
GND
+5V
/RST
/LDMEM
/ENMEM
/IO
/IRQ2
/IRQ3
DBUS0
DBUS1
DBUS2
DBUS3
DBUS4
DBUS5
DBUS6
DBUS7
ABUS0
ABUS1
ABUS2
ABUS3
ABUS4
ABUS5
ABUS6
ABUS7
ABUS8
ABUS9
ABUS10
ABUS11
ABUS12
ABUS13
ABUS14
ABUS15
IC5A
74LS04N
IC5B
74LS04N
IC5C
74LS04N
IC11
74LS245N
IDBUS0
IDBUS1
IDBUS2
IDBUS3
IDBUS4
IDBUS5
IDBUS6
IDBUS7
IDBUS02
IDBUS13
IDBUS24
IDBUS35
IDBUS46
IDBUS57
IDBUS68
IDBUS79
RN1
4k7
QG11.8432MHz
IC10B
74LS08N
IC10A
74LS08N
IC9A
74LS02N
IC9B
74LS02N
IC8
74LS138N
IC1
16C550
IC2
16C550
IC3
MAX232
IC4
MAX232
IC6
MAX232
IC7
MAX232
X1
X2
TX0
RTS0
CTS0
RX0
DTR0
DCD0
DSR0
TX1
RTS1
CTS1
RX1
DTR1
DCD1
DSR1
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
1uF
C27
10uF
C28
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
100n
IC9C
74LS02N
IC9D
74LS02N
IC10C
74LS08N
IC10D
74LS08N
IC5D
74LS04N
IC5E
74LS04N
IC5F
74LS04N
I/O - UARTS
Dawid Pilawa
(C) 2010 - 2012
TITLE: io_uarts
Document Number:
IO.1
REV:
1.0.3
Date: 2012-05-05 00:00:19
Sheet: 1/1


J1
DIN41612
GND
+5V
/IRQ1
/IRQ7
/IO
/RST
/LDMEM
/ENMEM
DBUS0
DBUS1
DBUS2
DBUS3
DBUS4
DBUS5
DBUS6
DBUS7
ABUS0
ABUS1
ABUS2
ABUS3
ABUS4
ABUS5
ABUS6
ABUS7
ABUS8
ABUS9
ABUS10
ABUS11
ABUS12
ABUS13
ABUS14
ABUS15
IC1
BQ4845
B1
CR2032
Q1
32.768kHz
R10
10k
IC2
74LS245N
DIR
G
RN1
4k7
IDBUS0
IDBUS1
IDBUS2
IDBUS3
IDBUS4
IDBUS5
IDBUS6
IDBUS7
IDBUS02
IDBUS13
IDBUS24
IDBUS35
IDBUS46
IDBUS57
IDBUS68
IDBUS79
74LS04N
IC11A
R2
10k
R5
2k2
R6
2k2
R7
2k2
R1
400
LED1
R8
2k2
R9
2k2
R3
2k2
R4
2k2
IC11B
IC5A
74LS32N
/CS1
IC5B
/CS0
IC5C
IC5D
IC10B
IC10C
74LS08N
IC7A
IC7B
SV1
DASP
/ENMEM
/LDMEM
IC9A
74LS02N
IC10A
IC9B
IC8
74LS138N
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
IC3
IC4
74LS374N
OC
CLK
IC6
74LS245N
RN2
RN3
IC10D
IC7C
IC7D
IC11C
IC11D
IC11E
IC11F
IC9C
IC9D
74LS02N
C11
10uF
C1
100n
C2
C3
C4
C5
C6
C7
C8
C9
C10
C12
I/O - IDE & RTC
Dawid Pilawa
(C) 2010, 2011
TITLE: io_rtc_ide
Document Number:
IO.2
REV:
1.0
Date: 2012-02-16 21:51:50
Sheet: 1/1