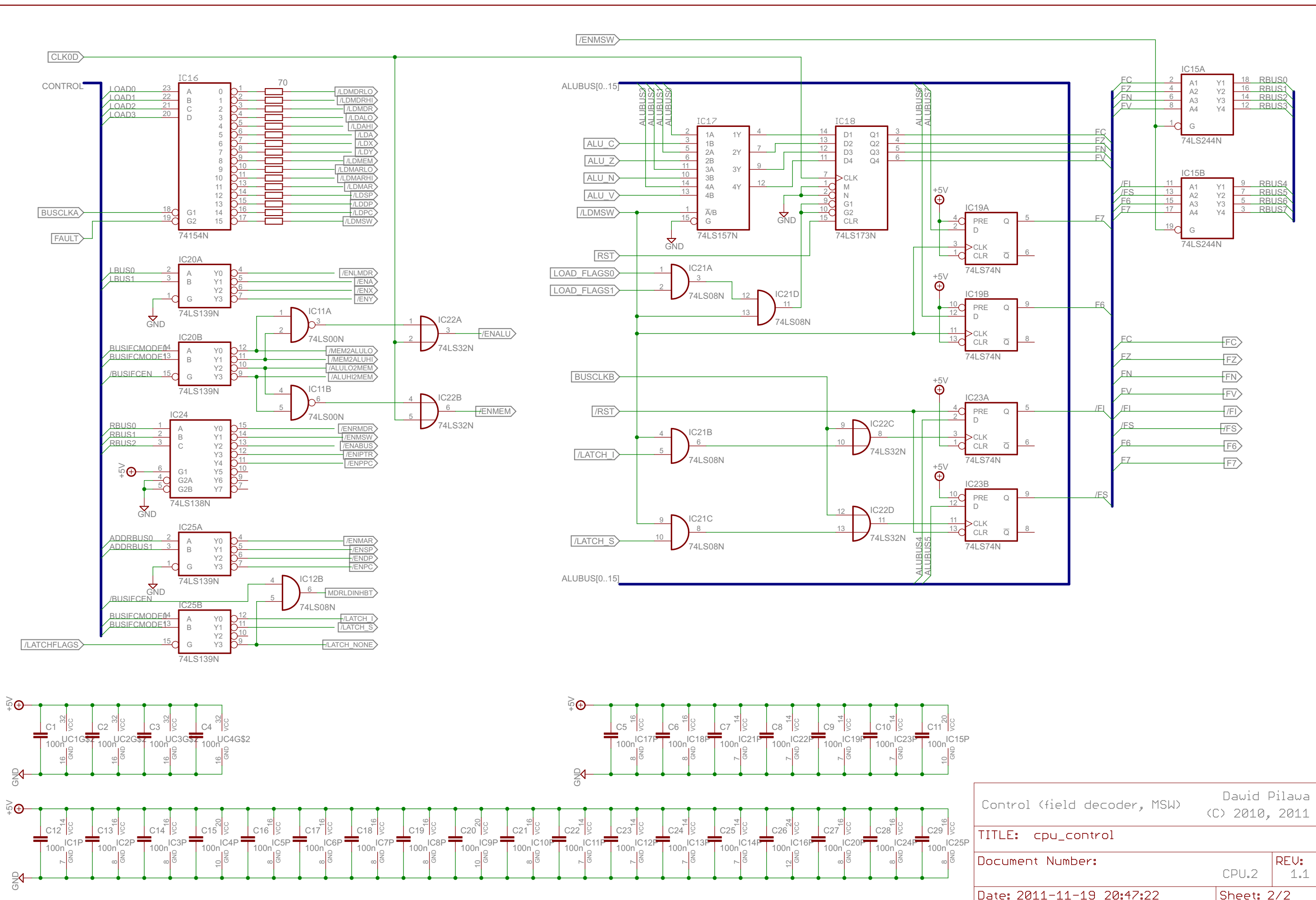


Control (microcode sequencer) Dawid Pilawa	
(C) 2010, 2011	
TITLE: cpu_control	
Document Number:	REV: 1.1
CPU.1	
Date: 2011-11-19 20:47:22	Sheet: 1/2

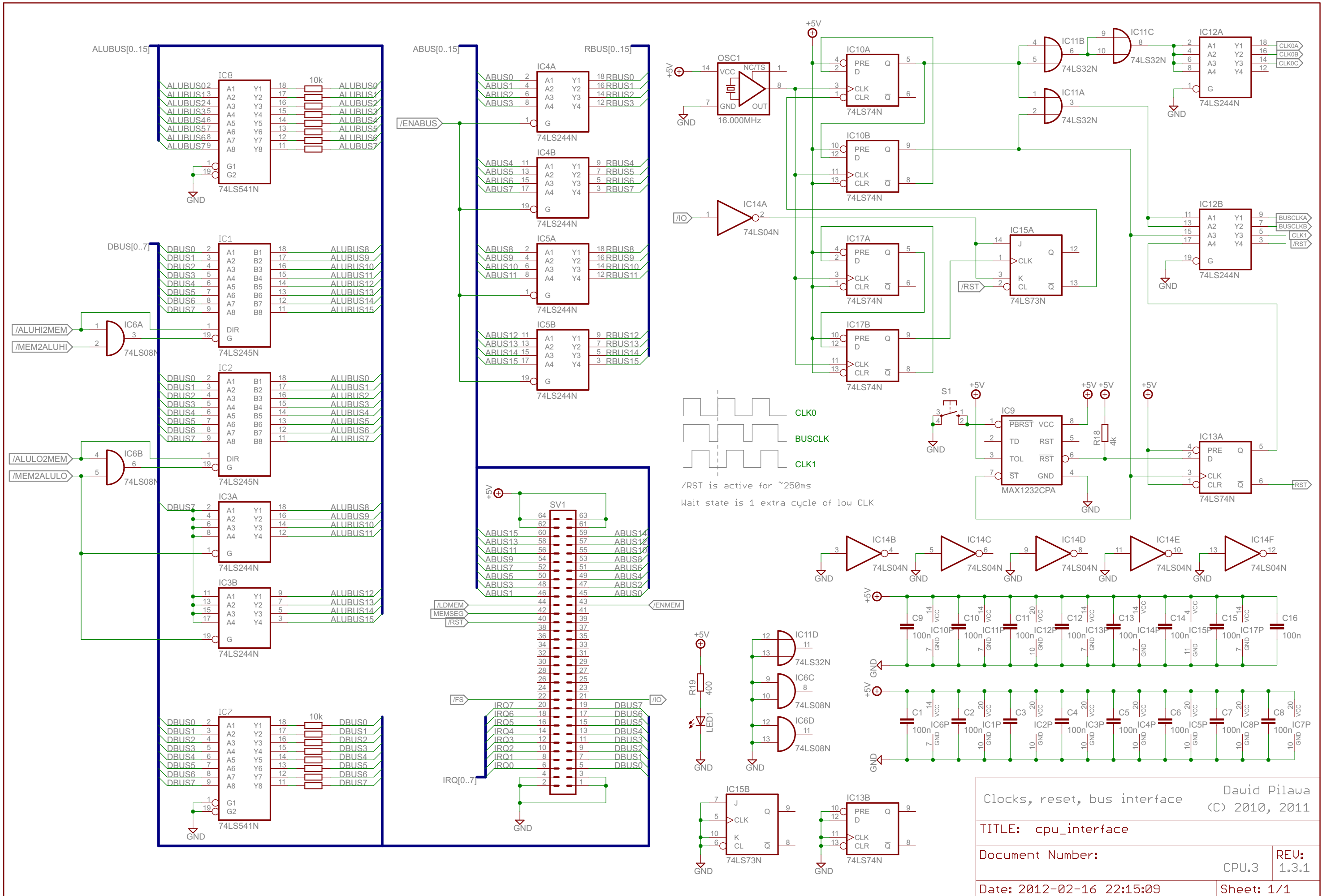


Control (field decoder, MSW) Dawid Pilawa
(C) 2010, 2011

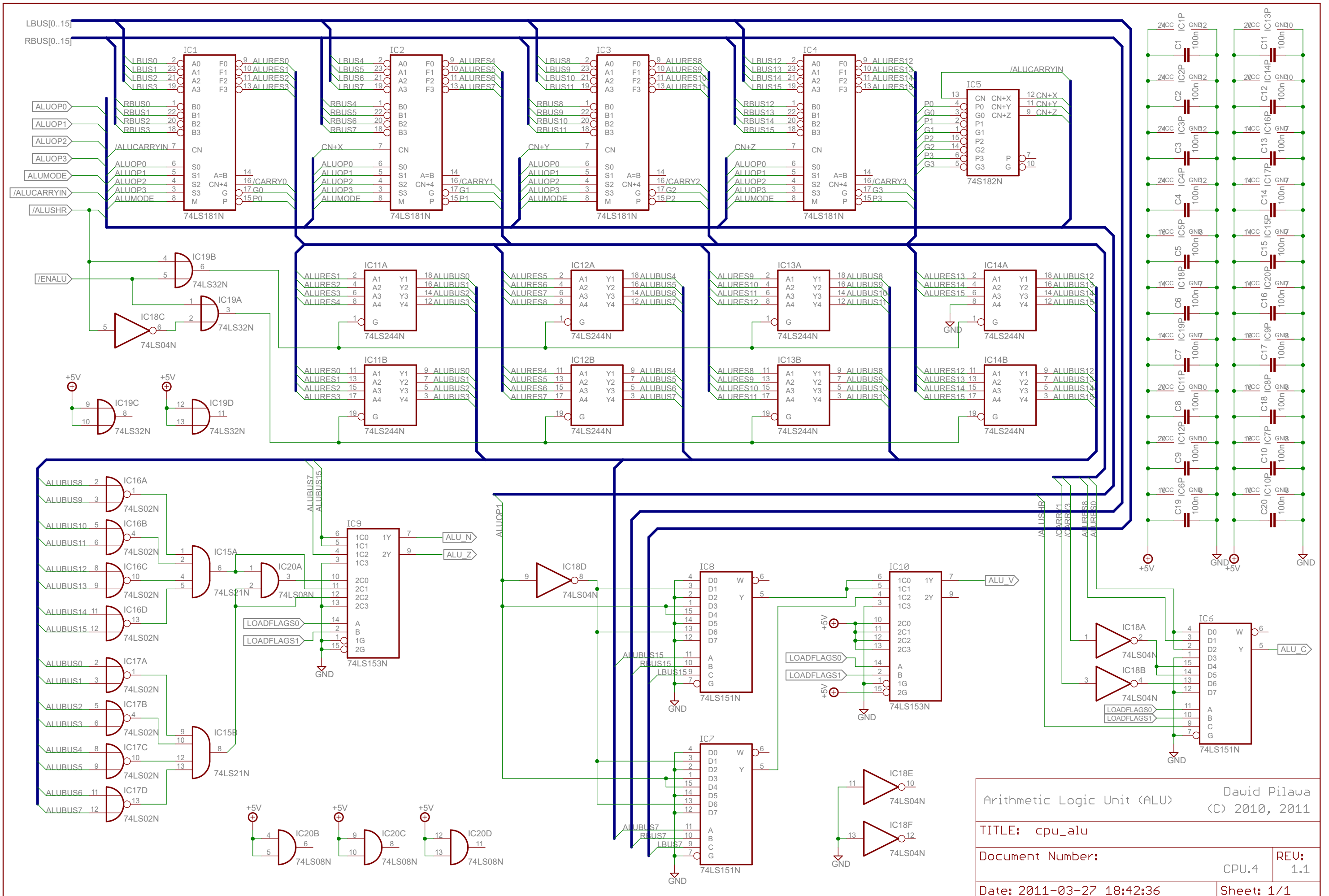
TITLE: cpu_control

Document Number: REV: 1.1

Date: 2011-11-19 20:47:22 CPU.2 Sheet: 2/2



Clocks, reset, bus interface Dawid Pilawa
(C) 2010, 2011
TITLE: cpu_interface
Document Number: CPU.3 **REV:** 1.3.1
Date: 2012-02-16 22:15:09 **Sheet:** 1/1

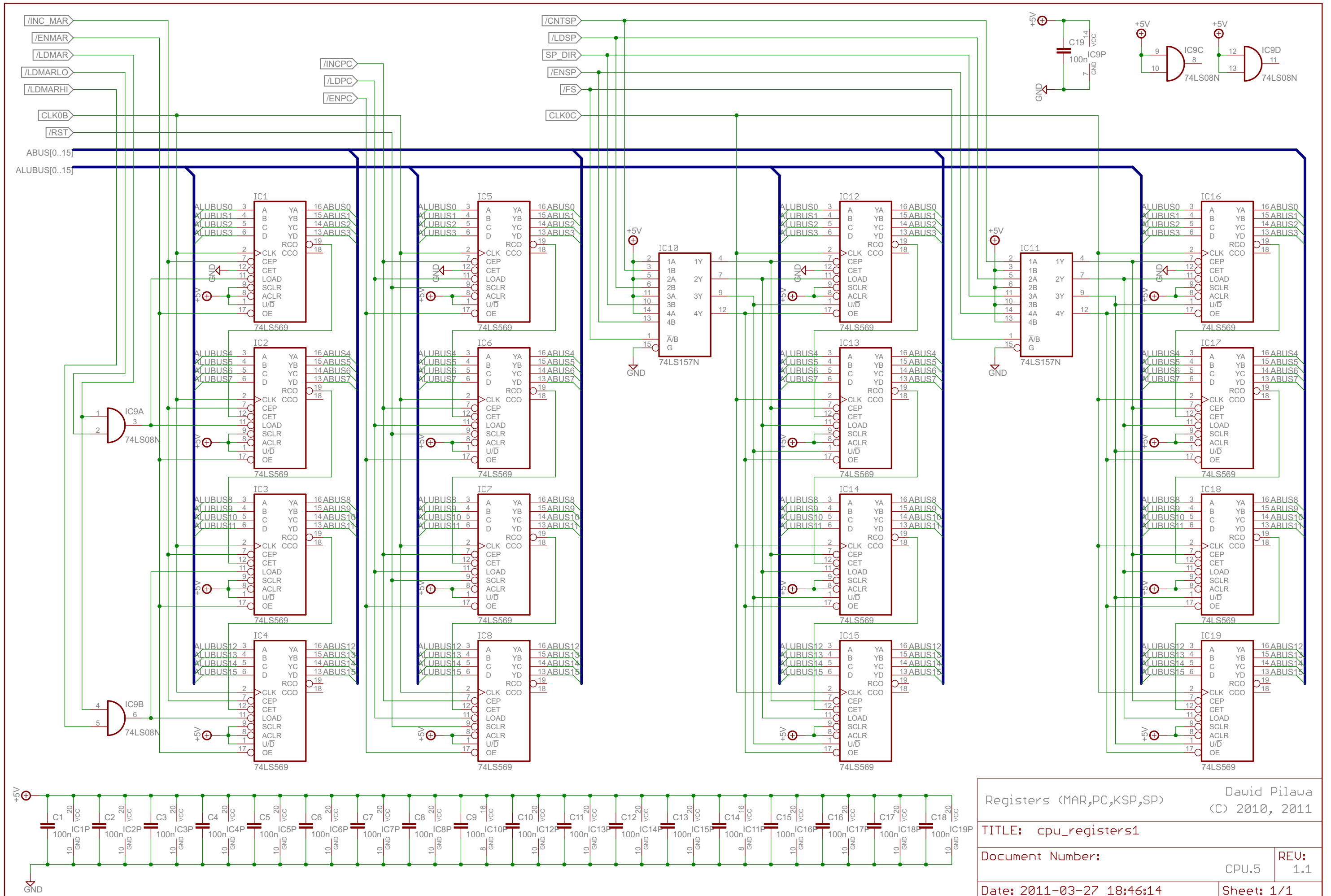


Arithmetic Logic Unit (ALU) Dawid Pilawa
(C) 2010, 2011

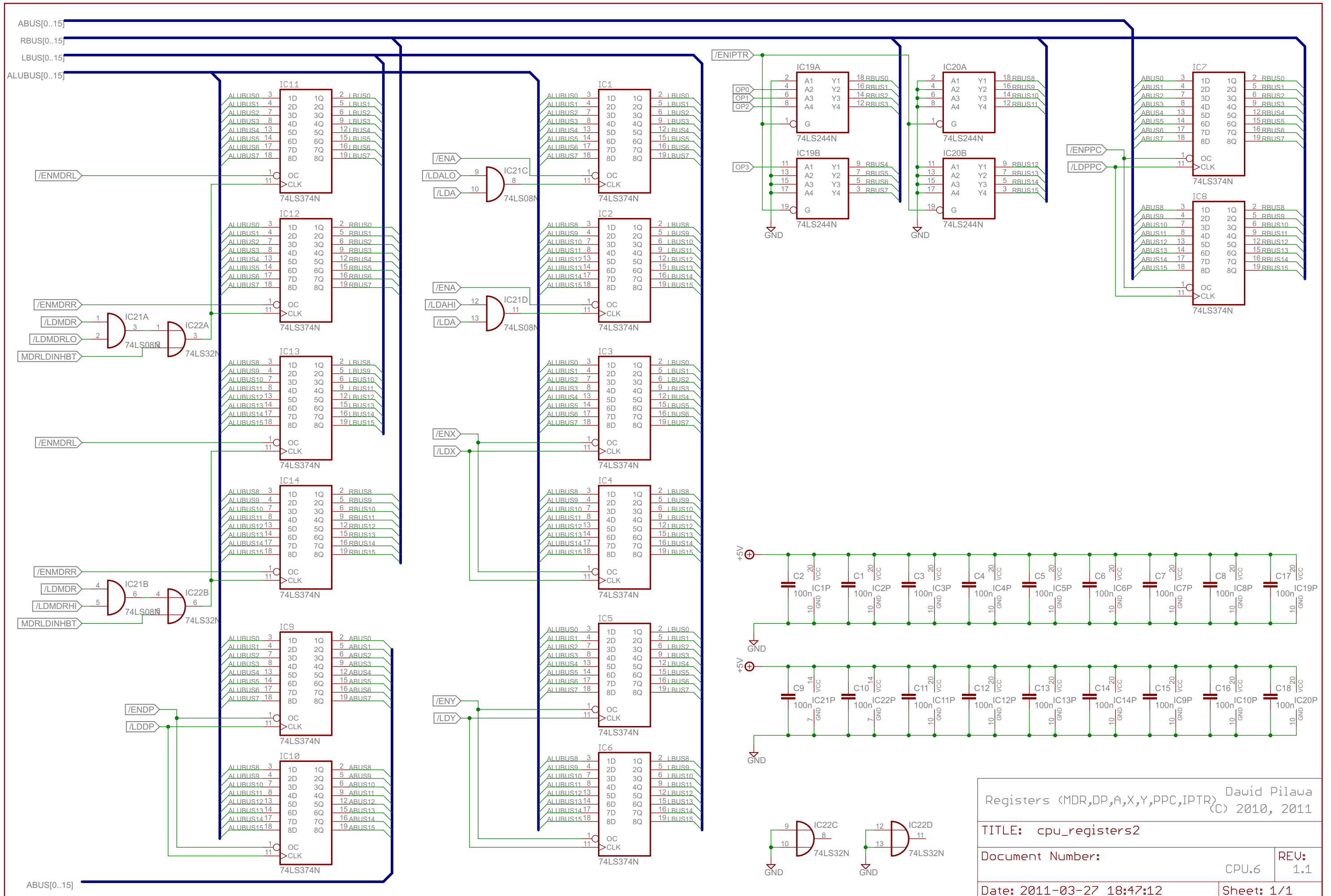
TITLE: cpu_alu

Document Number: CPU.4 REV: 1.1

Date: 2011-03-27 18:42:36 Sheet: 1/1



Registers (MAR,PC,KSP,SP)		Dawid Pilawa	
		(C) 2010, 2011	
TITLE: cpu_registers1			
Document Number:		REV: 1.1	
		CPU.5	
Date: 2011-03-27 18:46:14		Sheet: 1/1	

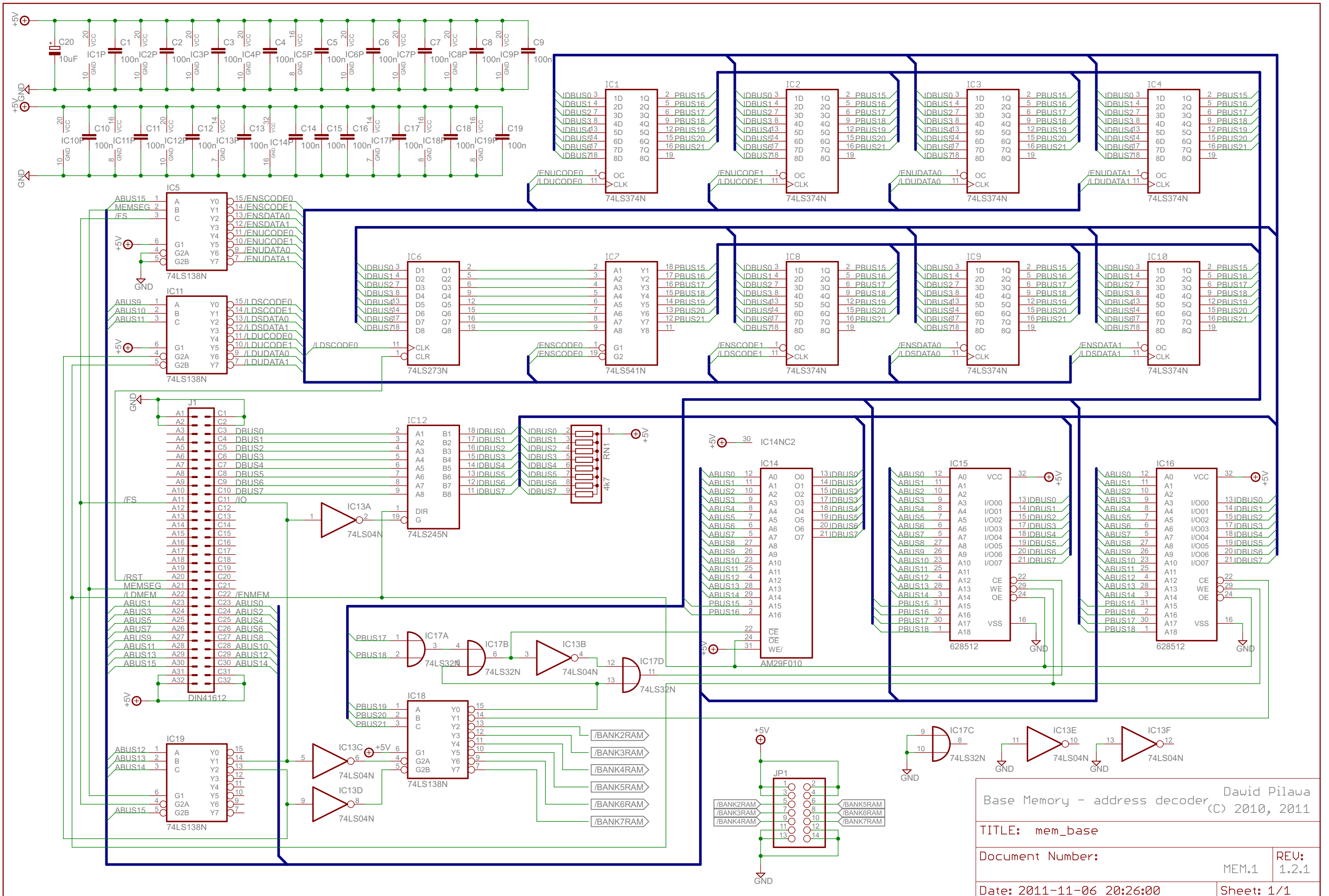


Dawid Pilawa
(C) 2010, 2011

TITLE: cpu_registers2

Document Number: CPU.6 REV: 1.1

Date: 2011-03-27 18:47:12 Sheet: 1/1



Base Memory - address decoder, Dawid Pilawa
 (C) 2010, 2011

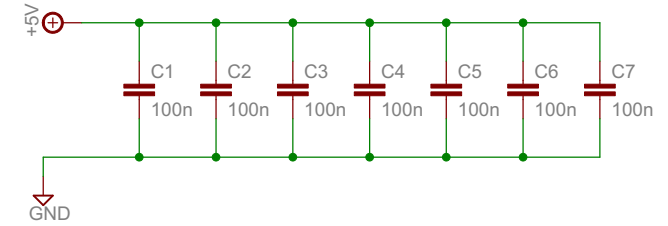
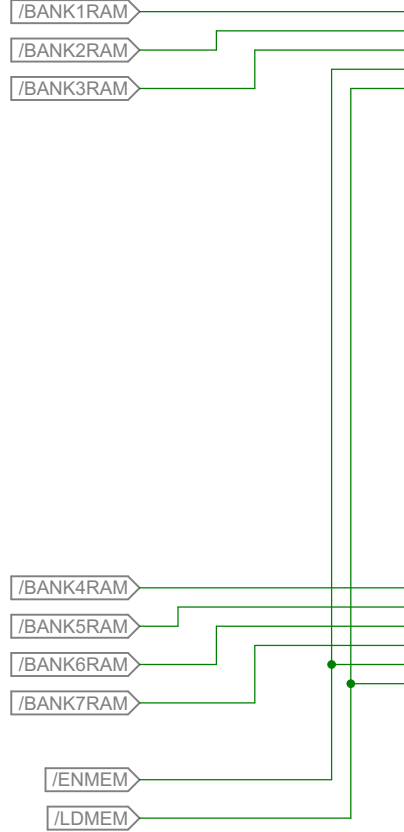
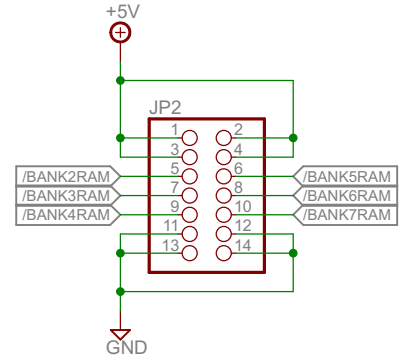
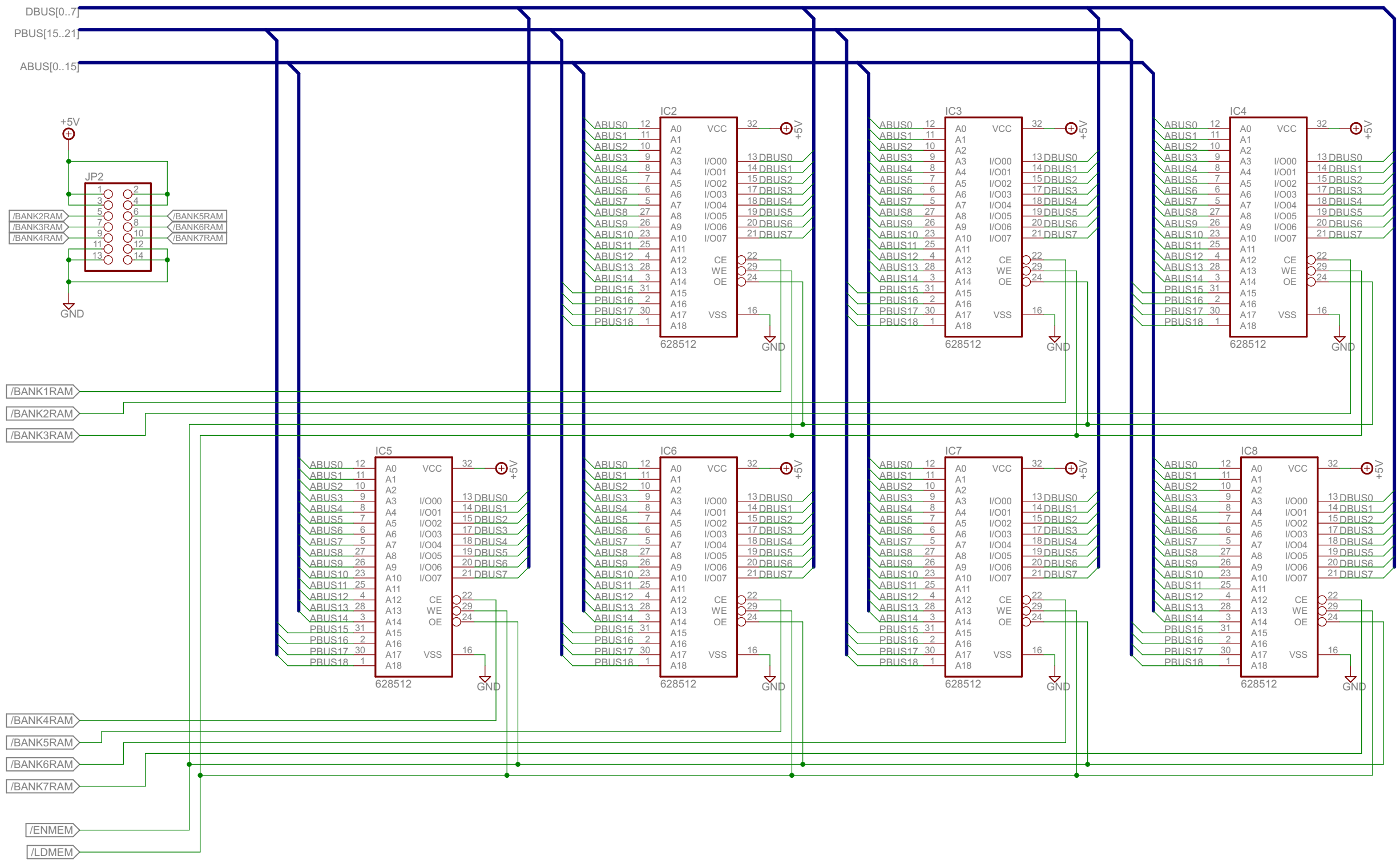
TITLE: mem_base

Document Number: MEM.1

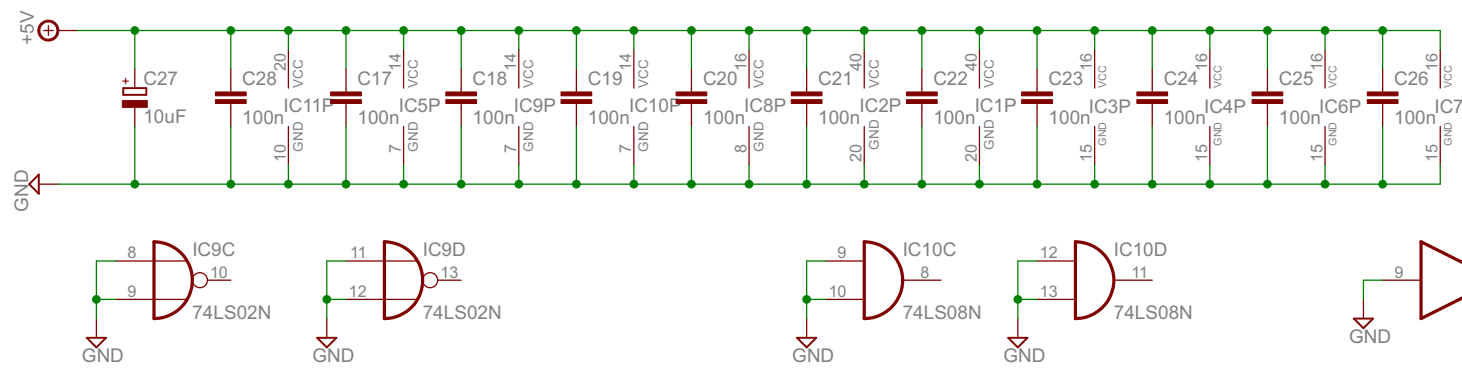
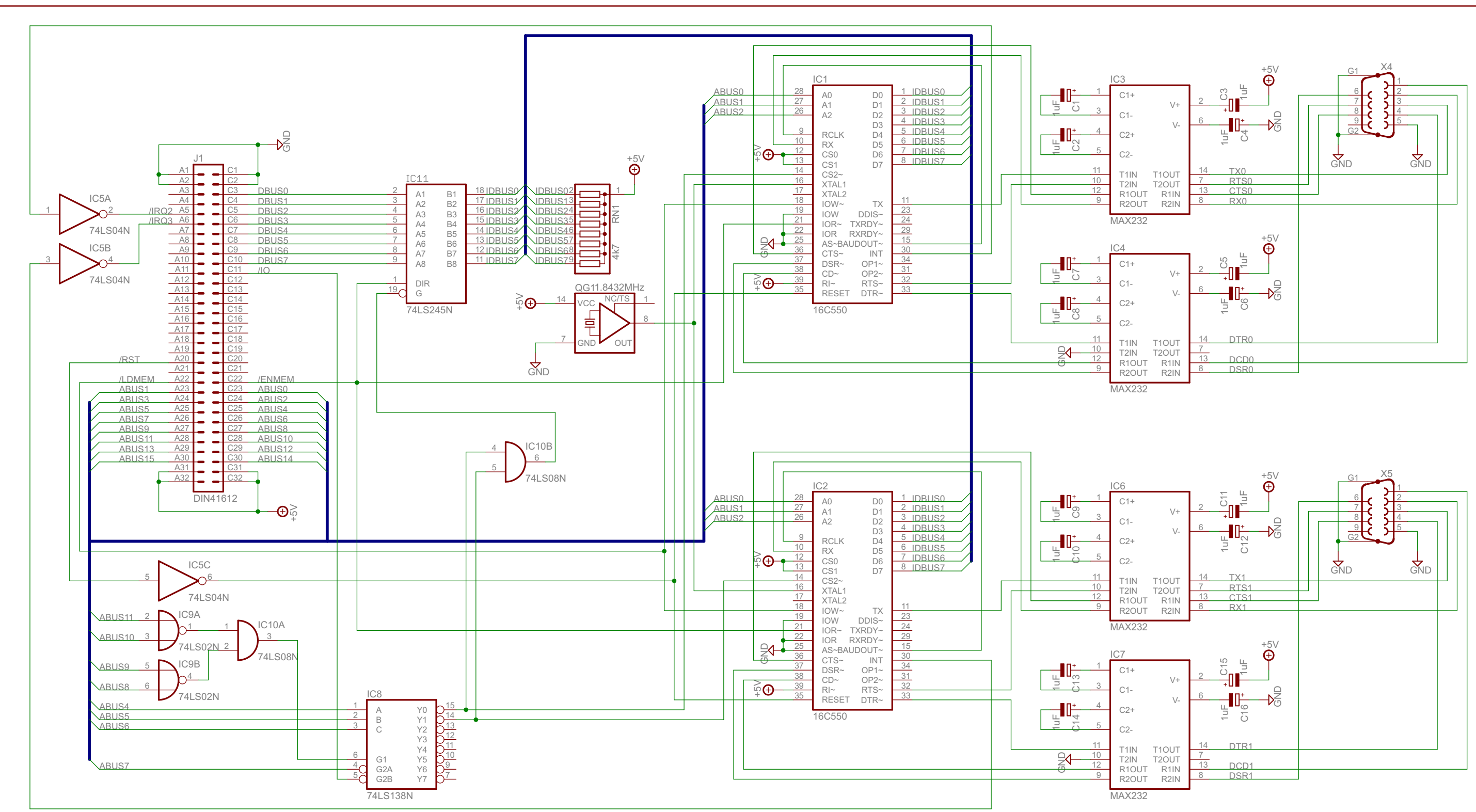
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REU: 1.2.1

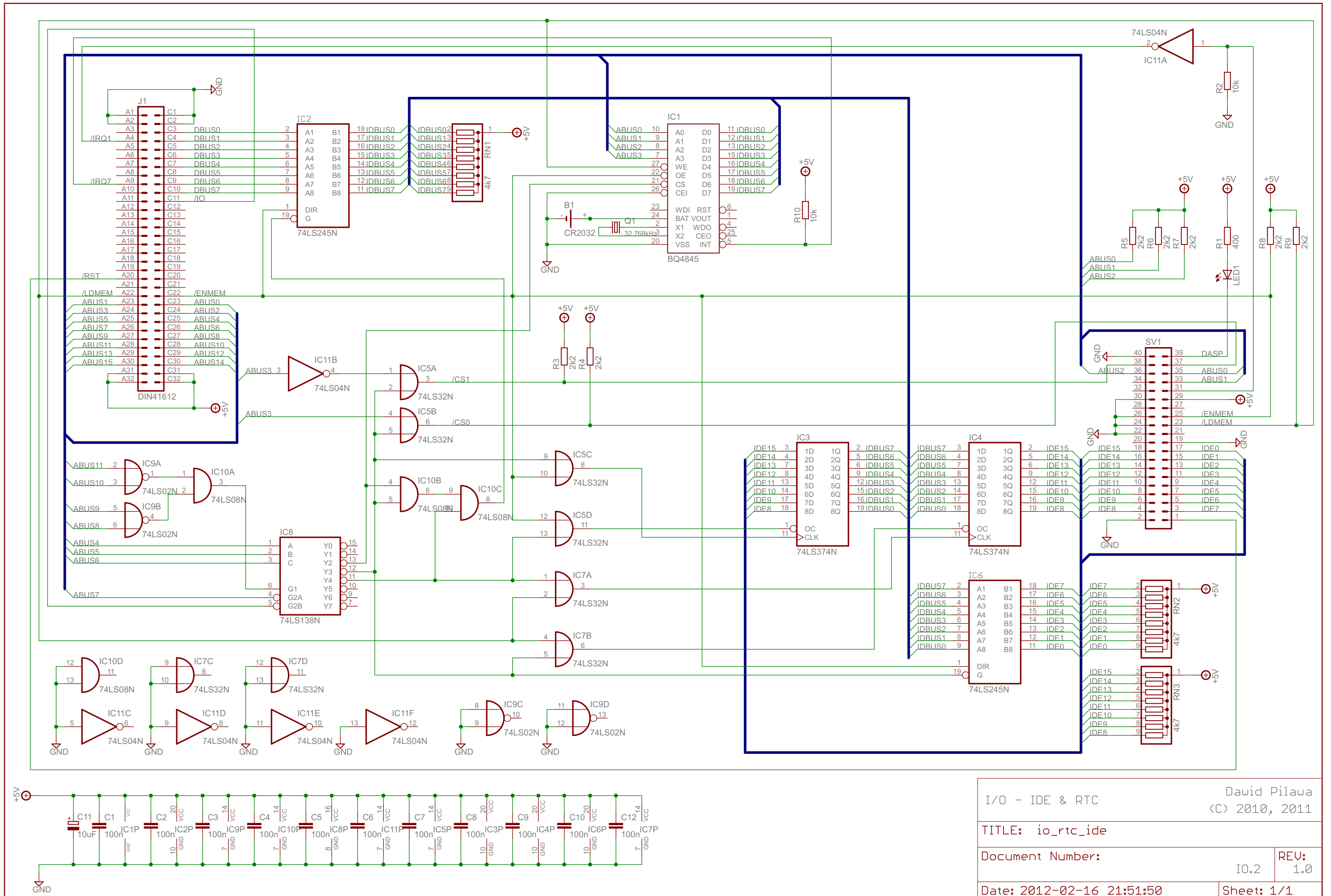
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Extended Memory		Dawid Pilawa (C) 2010, 2011	
TITLE: mem_ext			
Document Number:		MEM.2	REV: 1.2.1
Date: 2012-01-08 17:41:52		Sheet: 1/1	



I/O - UARTS		Dawid Pilawa	
		(C) 2010, 2011	
TITLE: io_uartS			
Document Number:		10.1	REV: 1.0.2
Date: 2011-10-22 22:44:12			Sheet: 1/1



I/O - IDE & RTC		Dawid Pilawa	
		(C) 2010, 2011	
TITLE: io_rtc_ide			
Document Number:		REV: 1.0	
		10.2	
Date: 2012-02-16 21:51:50		Sheet: 1/1	