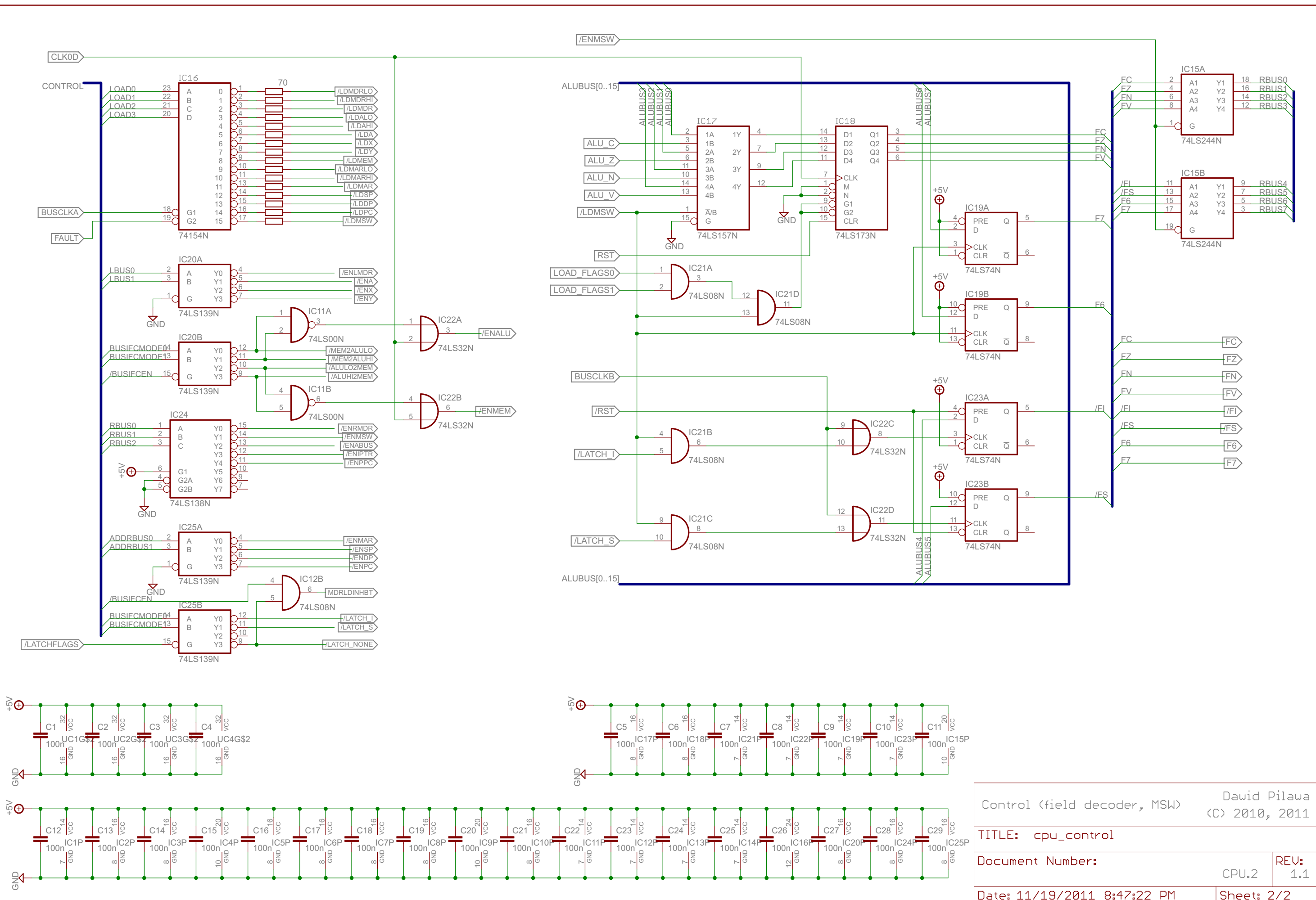
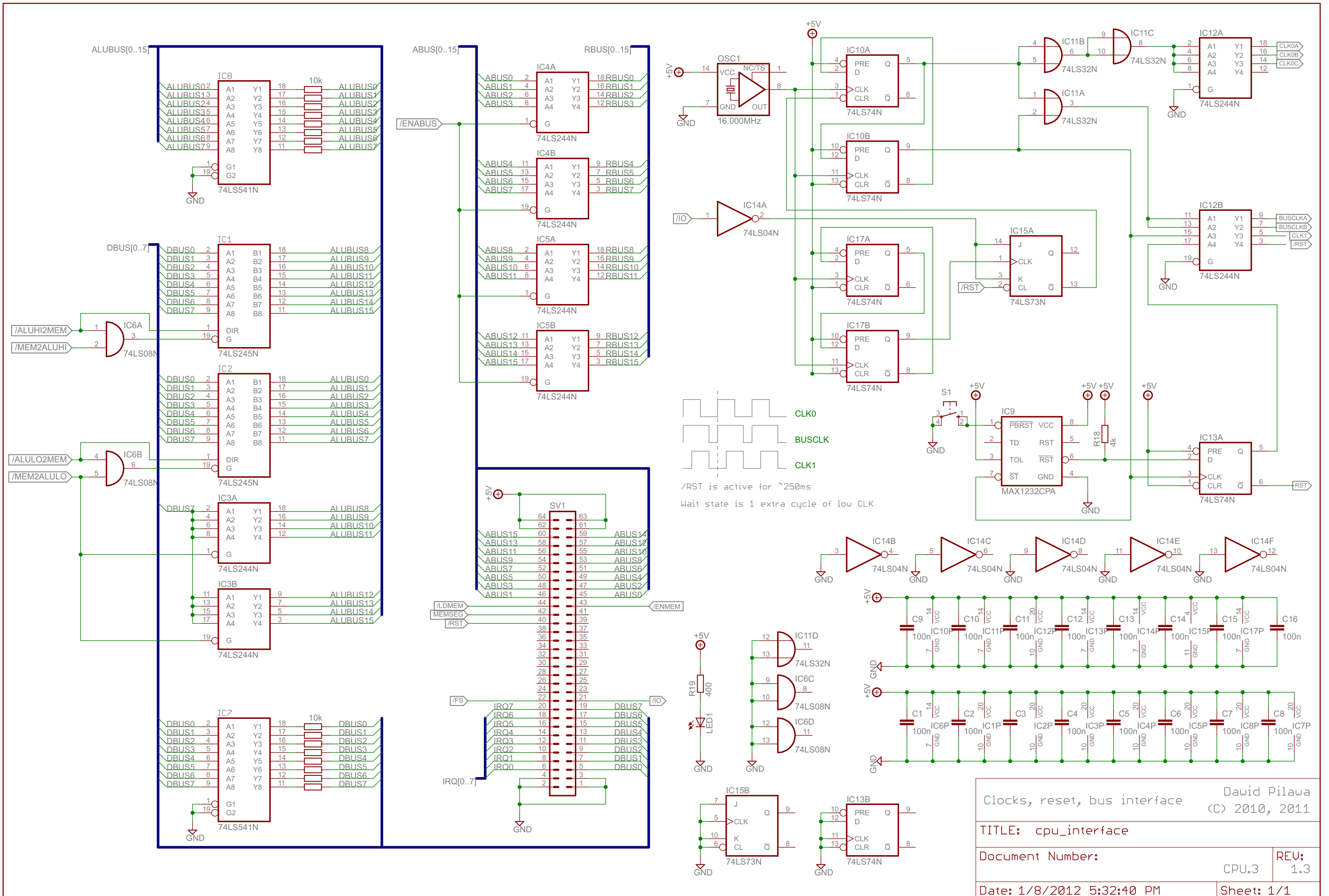


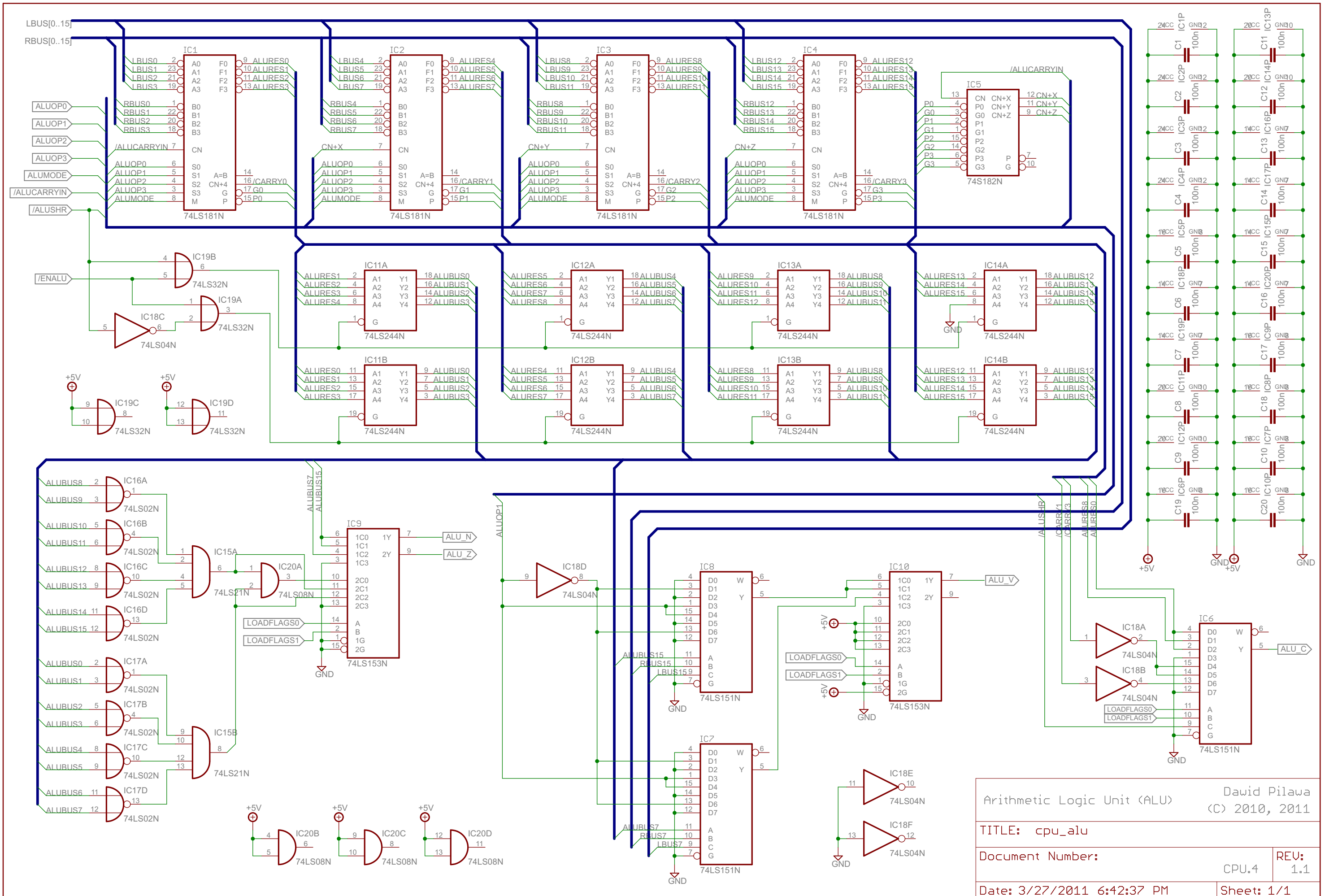
Control (microcode sequencer) Dawid Pilawa (C) 2010, 2011	
TITLE: cpu_control	
Document Number:	REV: 1.1
Date: 11/19/2011 8:47:22 PM	Sheet: 1/2



Control (field decoder, MSW)		Dawid Pilawa	
		(C) 2010, 2011	
TITLE: cpu_control			
Document Number:		REV: 1.1	
		CPU.2	
Date: 11/19/2011 8:47:22 PM		Sheet: 2/2	



Clocks, reset, bus interface		Dawid Pilawa	
		(C) 2010, 2011	
TITLE: cpu_interface			
Document Number:		REV: 1.3	
Date: 1/8/2012 5:32:40 PM		CPU.3	
		Sheet: 1/1	



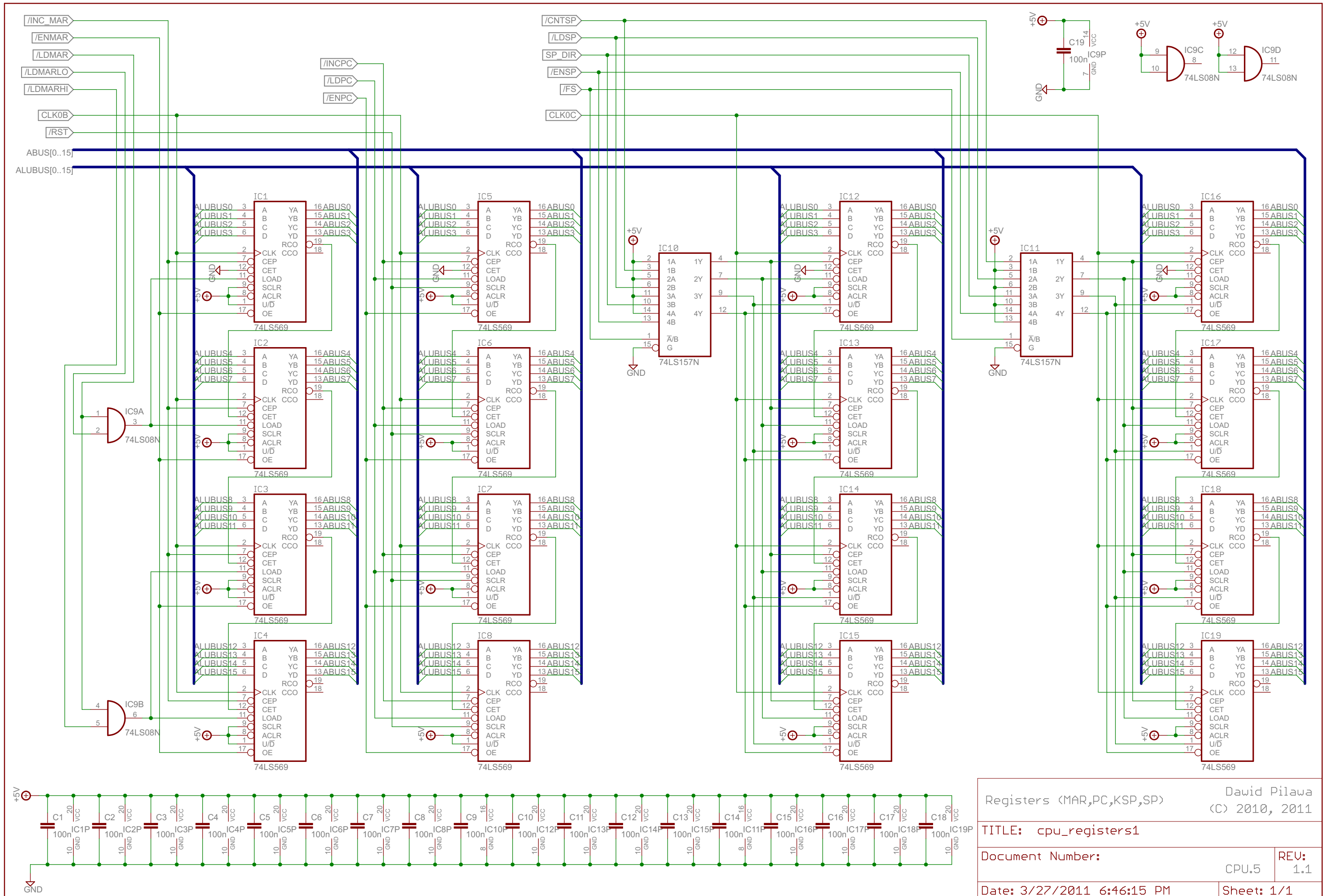
Arithmetic Logic Unit (ALU) Dawid Pilawa
(C) 2010, 2011

TITLE: cpu_alu

Document Number: REV: 1.1

Date: 3/27/2011 6:42:37 PM CPU.4

Sheet: 1/1



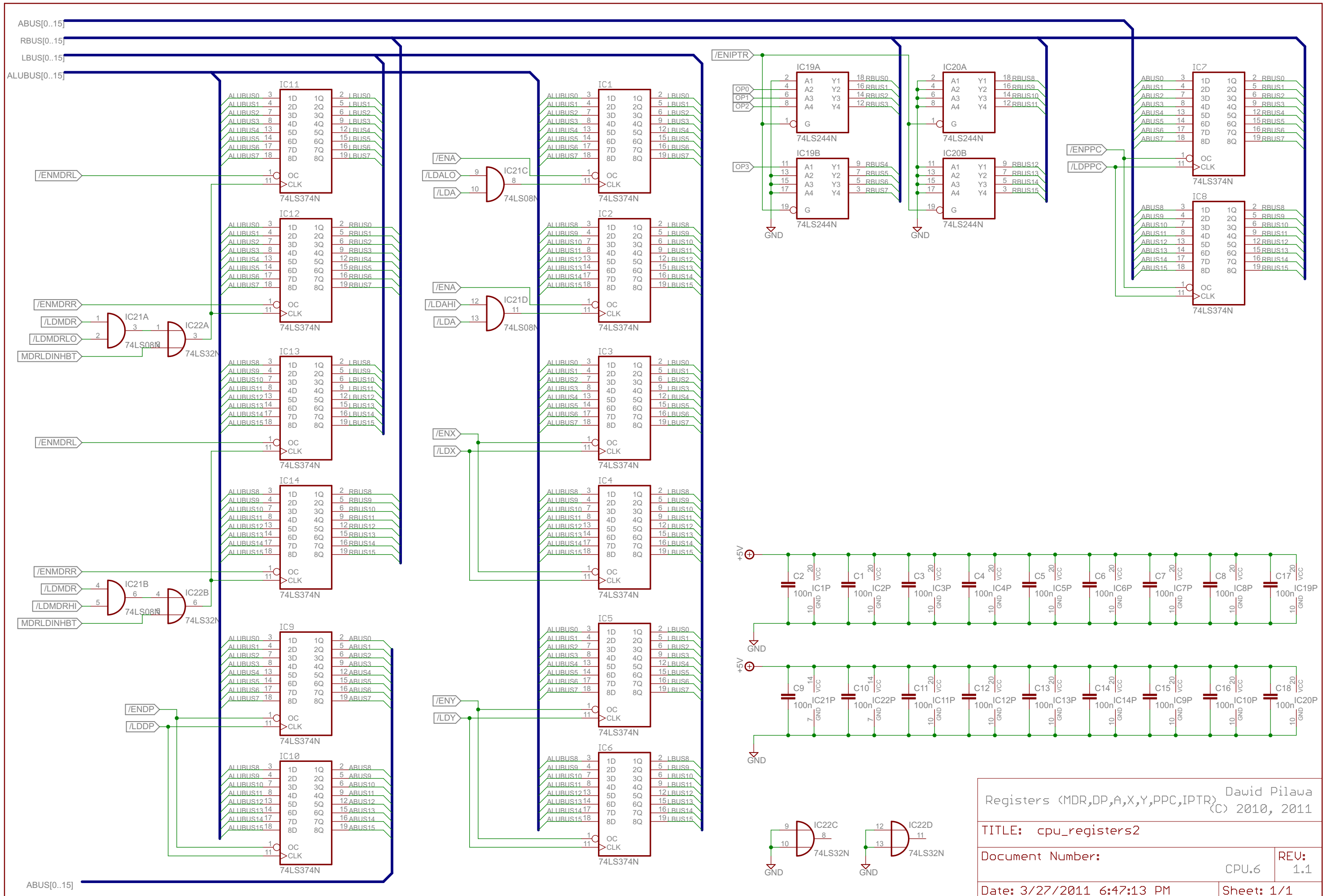
Registers (MAR,PC,KSP,SP) Dawid Pilawa
(C) 2010, 2011

TITLE: cpu_registers1

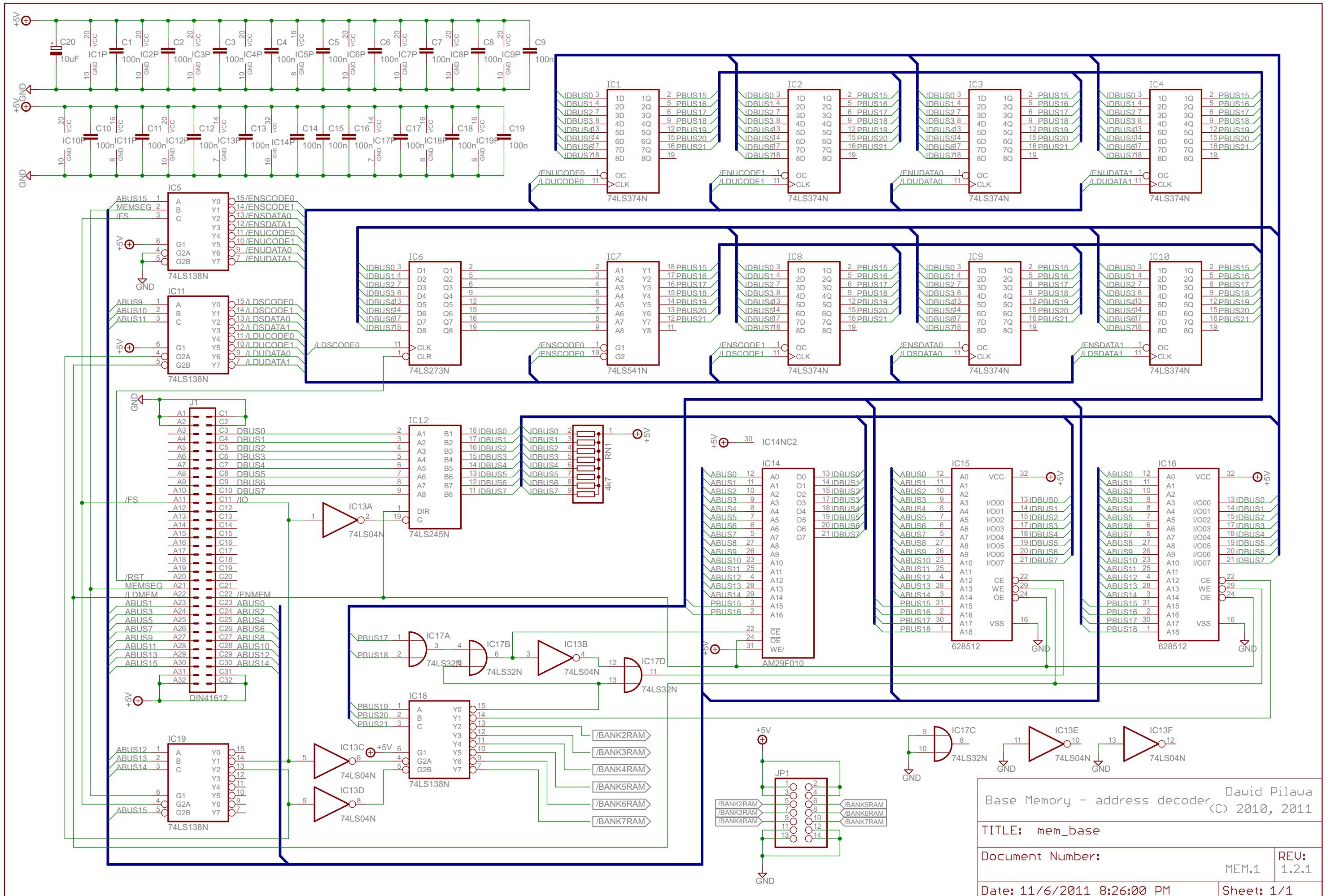
Document Number: REV: 1.1

Date: 3/27/2011 6:46:15 PM CPU.5

Sheet: 1/1



Registers (MDR,DP,A,X,Y,PPC,IPTR) Dawid Pilawa
 (C) 2010, 2011
 TITLE: cpu_registers2
 Document Number: CPU.6 REV: 1.1
 Date: 3/27/2011 6:47:13 PM Sheet: 1/1



Base Memory - address decoder, Daid Pilawa
 (C) 2010, 2011

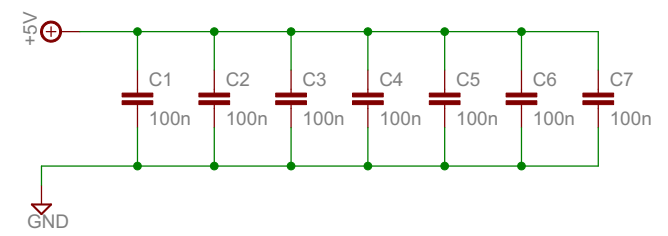
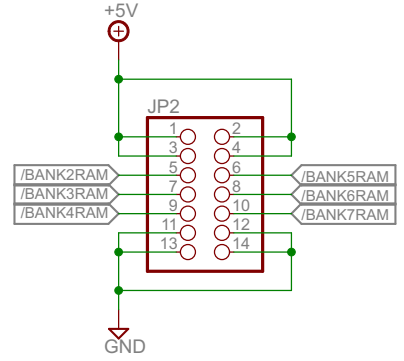
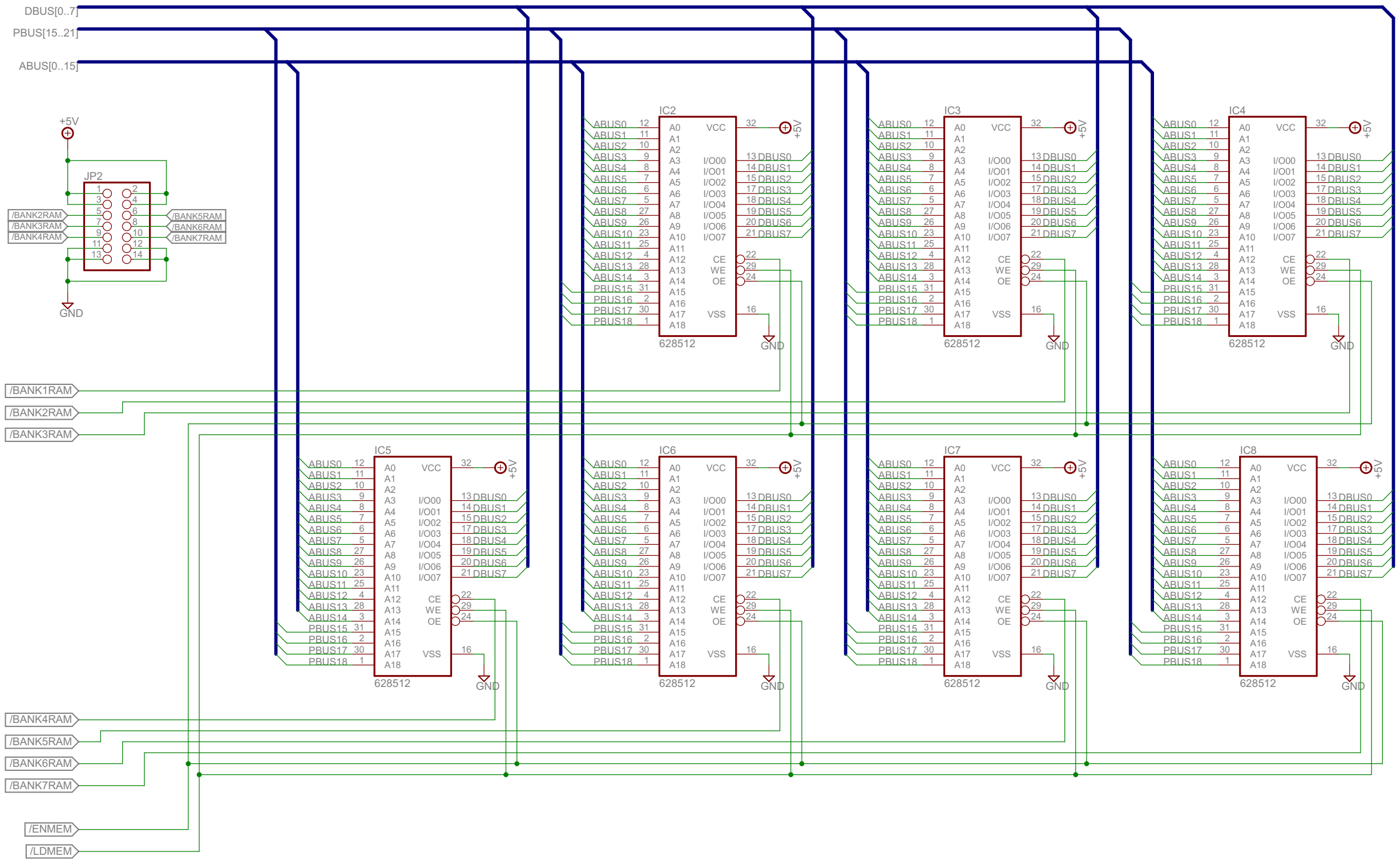
TITLE: mem_base

Document Number: MEM.1

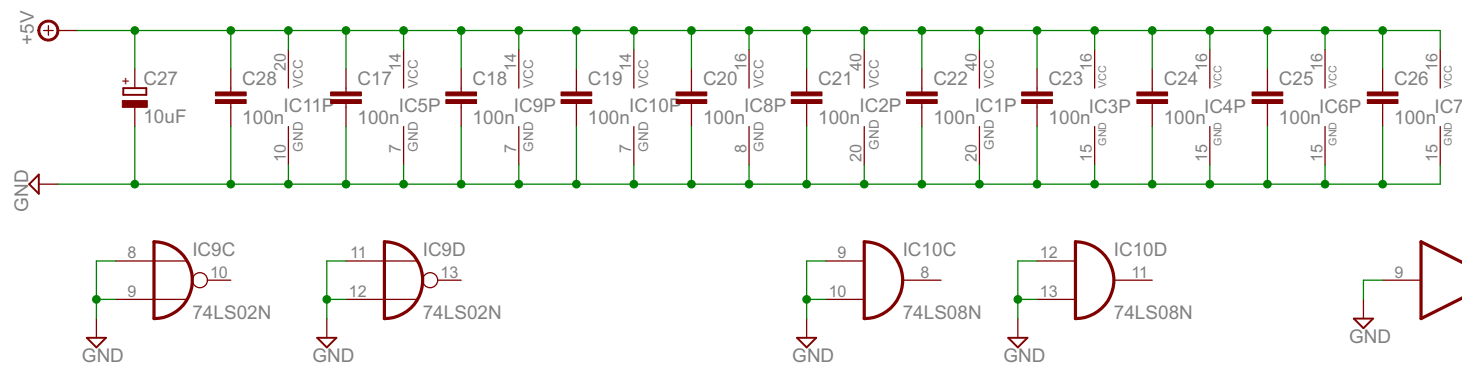
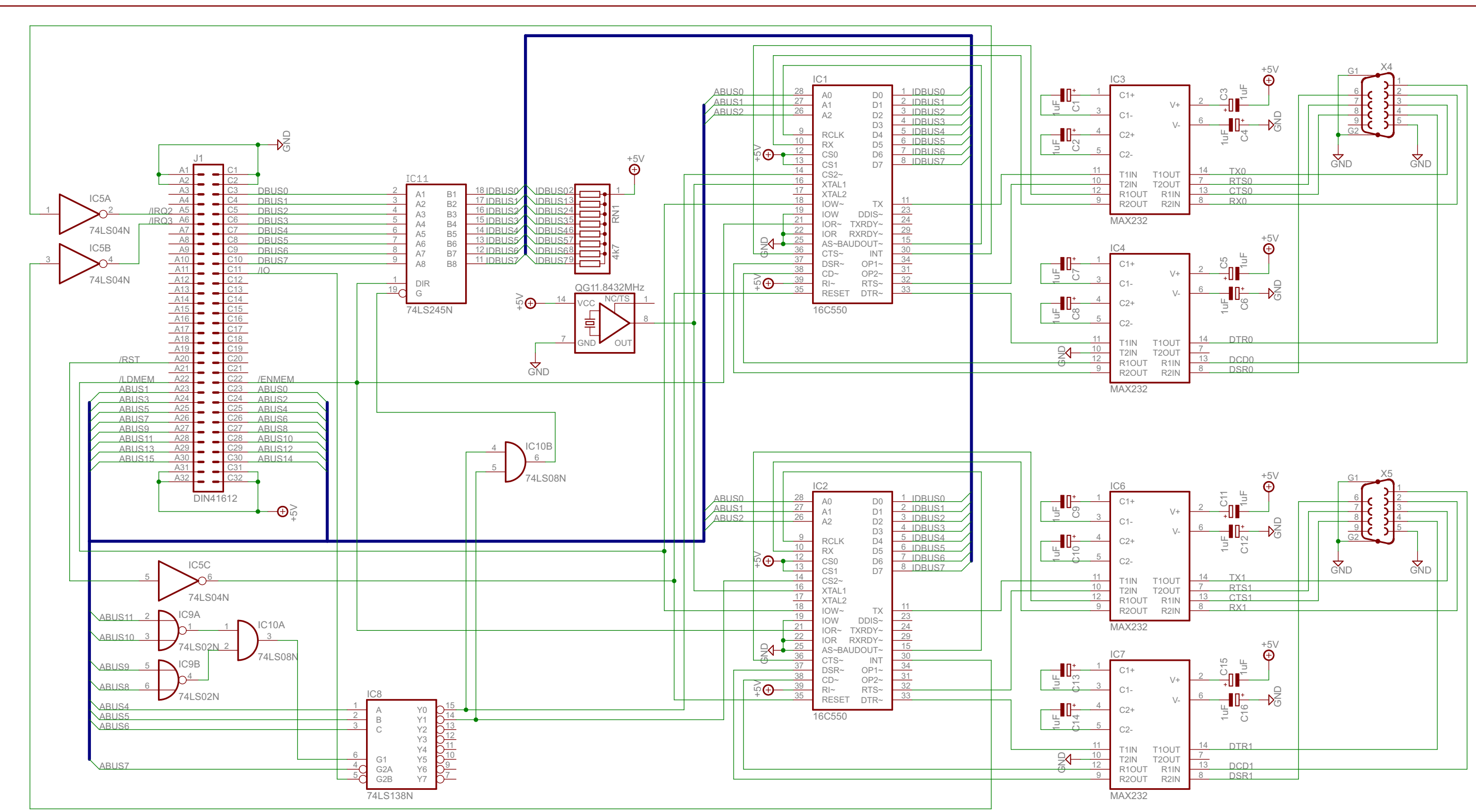
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REU: 1.2.1

Sheet: 1/1



Extended Memory		Dawid Pilawa (C) 2010, 2011	
TITLE: mem_ext			
Document Number:		MEM.2	REV: 1.2.1
Date: 1/8/2012 5:41:53 PM		Sheet: 1/1	



I/O - UARTS		Dawid Pilawa	
		(C) 2010, 2011	
TITLE: io_uartS			
Document Number:		10.1	REV: 1.0.2
Date: 10/22/2011 10:44:13 PM		Sheet: 1/1	