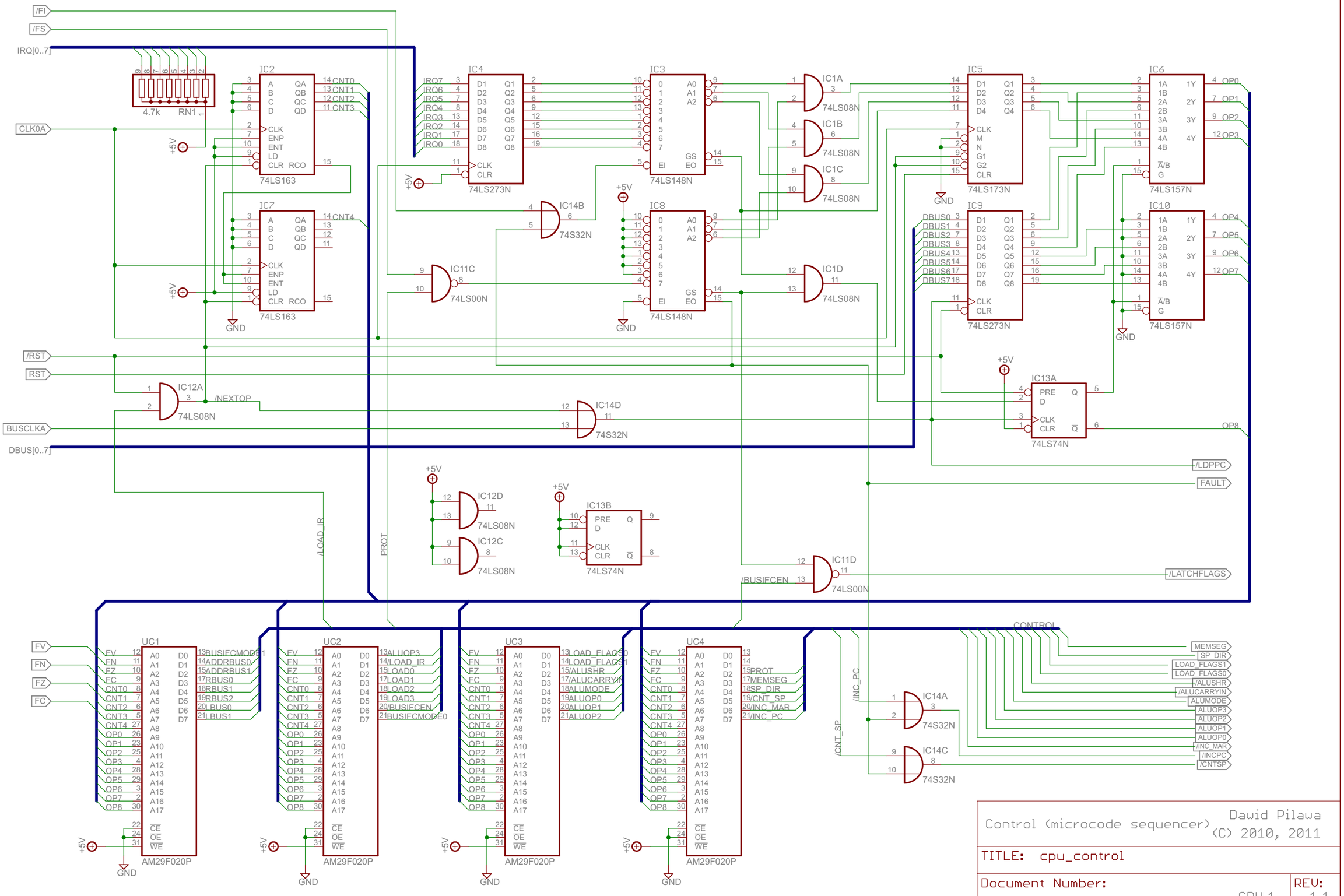


Control (microcode sequencer)

Dawid Pilawa
(C) 2010, 2011

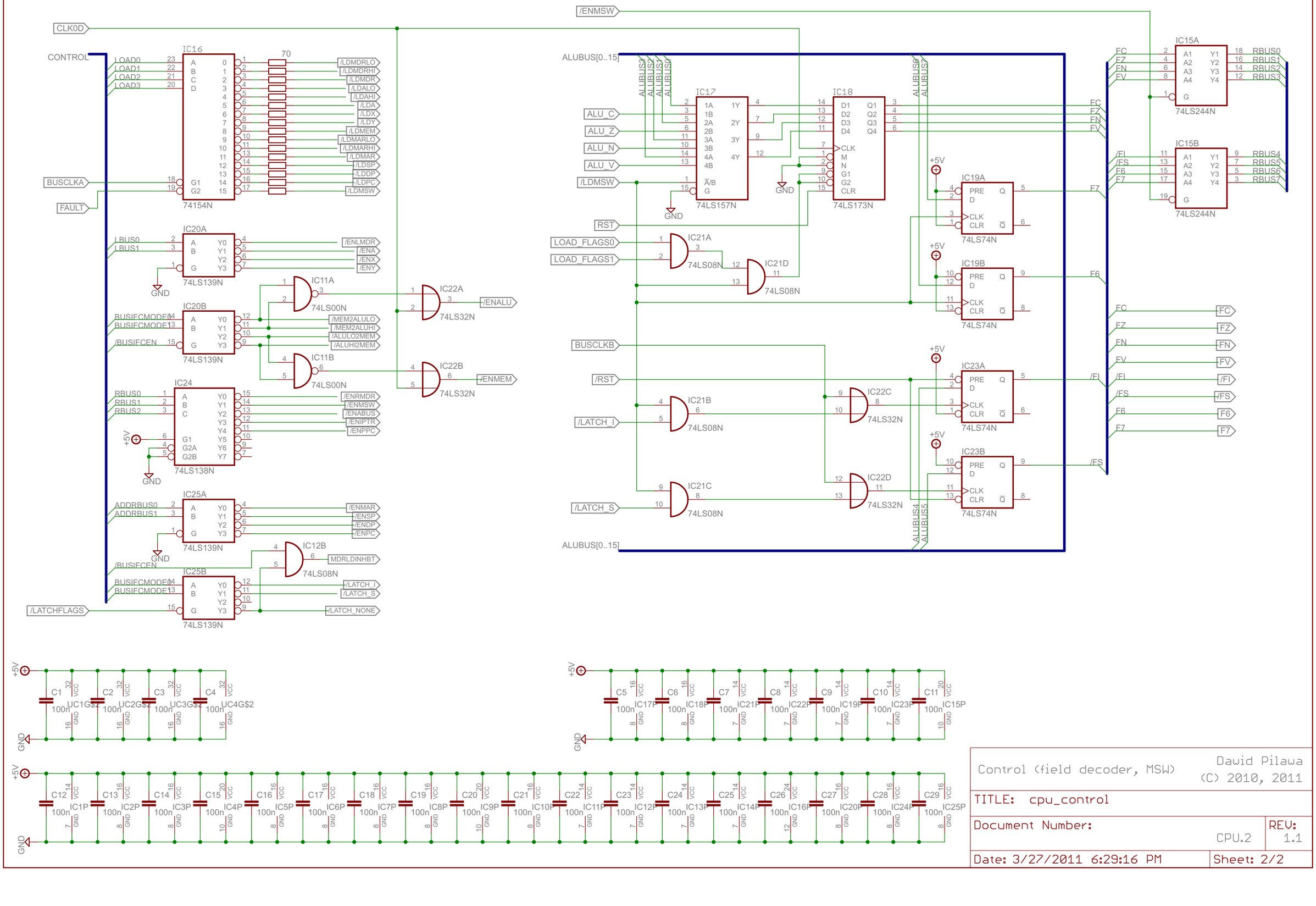
TITLE: cpu_control

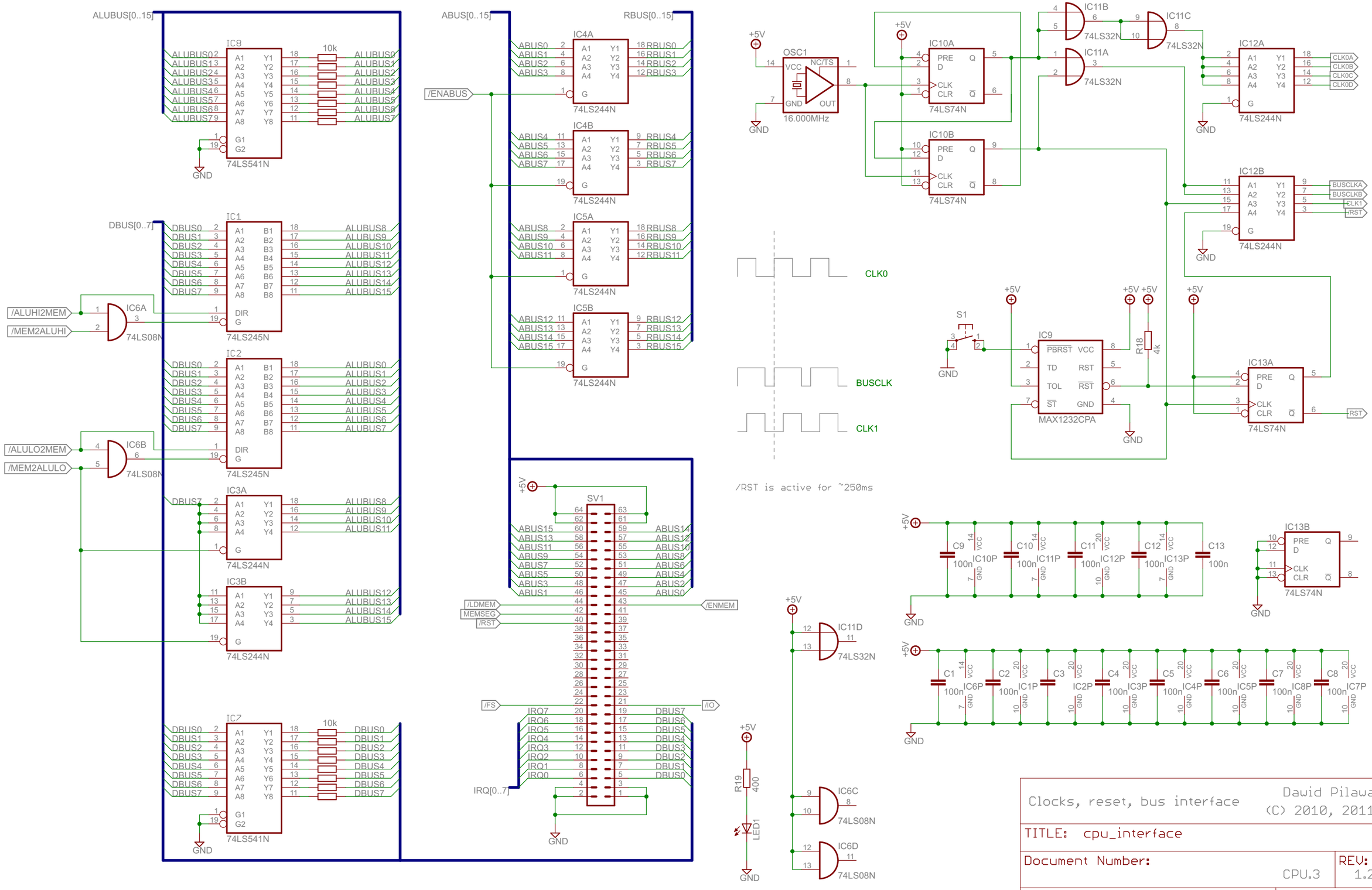
Document Number: CPU.1

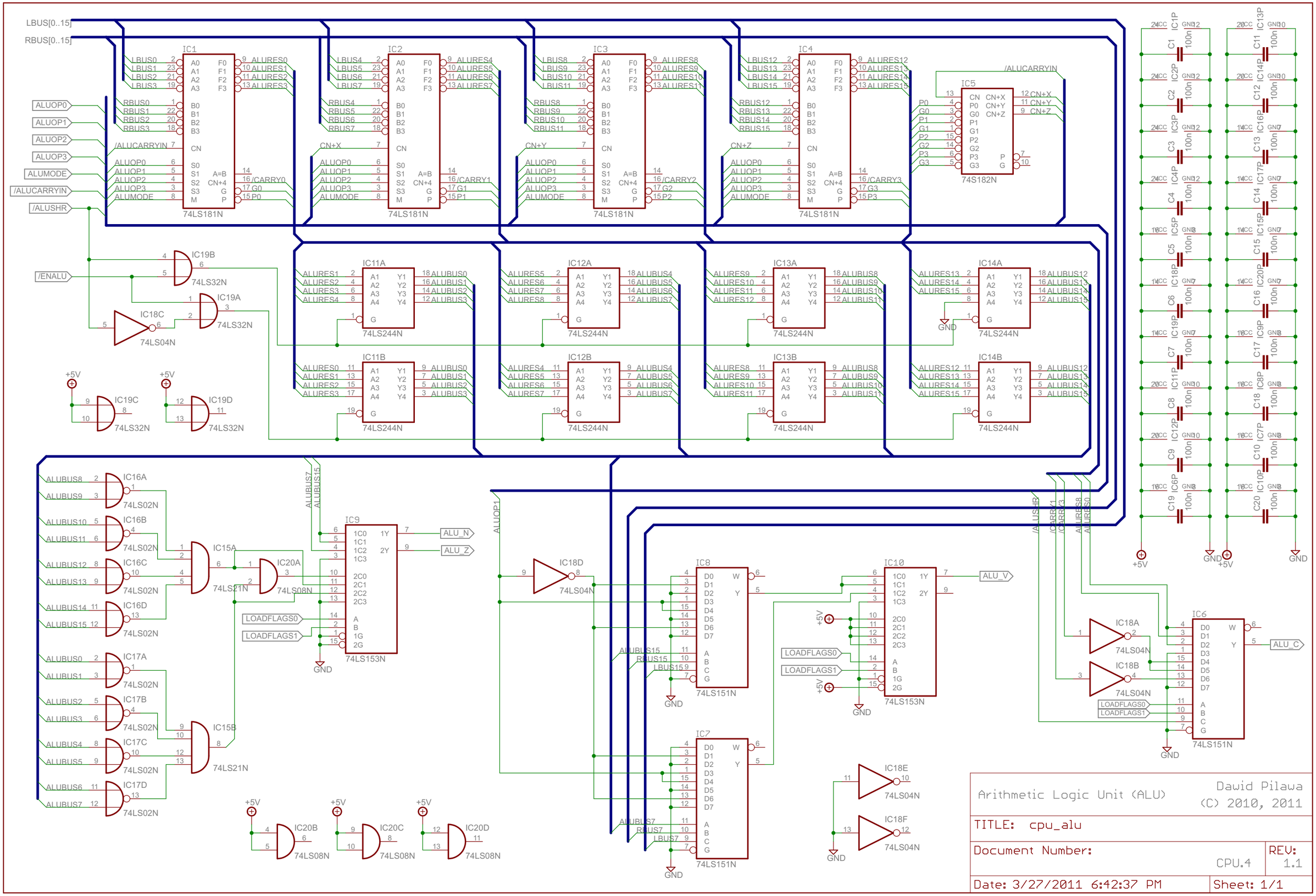
REV: 1.1

Date: 3/27/2011 6:29:16 PM

Sheet: 1/2


CLK0D
/ENMSW
CONTROL
ALUBUS[0..15]
IC16
74154N
70
/LDMDRLO
/LDMDRHI
/LDMDR
/LDALO
/LDAHI
/LDA
/LDX
/LDY
/LDMEM
/LDMARLO
/LDMARHI
/LDMAR
/LDSP
/LDDP
/LDPC
/LDMSW
LOAD0
LOAD1
LOAD2
LOAD3
BUSCLKA
FAULT
IC17
74LS157N
IC18
74LS173N
ALU_C
ALU_Z
ALU_N
ALU_V
/LDMSW
GND
RST
LOAD_FLAGS0
LOAD_FLAGS1
IC21A
IC21D
74LS08N
IC15A
IC15B
74LS244N
FC
FZ
FN
FV
/FI
/FS
F6
F7
RBUS0
RBUS1
RBUS2
RBUS3
RBUS4
RBUS5
RBUS6
RBUS7
+5V
IC19A
IC19B
74LS74N
IC20A
74LS139N
/ENLMDR
/ENA
/ENX
/ENY
IBUS0
IBUS1
IC11A
74LS00N
IC22A
74LS32N
/ENALU
IC20B
/MEM2ALULO
/MEM2ALUHI
/ALULO2MEM
/ALUHI2MEM
/BUSIFCEN
IC11B
IC22B
/ENMEM
BUSCLKB
/RST
/LATCH_I
IC21B
IC22C
IC23A
IC23B
IC24
74LS138N
/ENRMDR
/ENMSW
/ENABUS
/ENIPTR
/ENPPC
RBUS0
RBUS1
RBUS2
IC25A
/ENMAR
/ENSP
/ENDP
/ENPC
ADDRBUS0
ADDRBUS1
IC12B
MDRLDINHBT
IC25B
/LATCH_I
/LATCH_S
/LATCH_NONE
/LATCHFLAGS
IC21C
IC22D
/LATCH_S
ALUBUS4
ALUBUS5
ALUBUS6
ALUBUS7
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
100n
VCC
GND
Control (field decoder, MSW)
Dawid Pilawa
(C) 2010, 2011
TITLE: cpu_control
Document Number:
CPU.2
REV:
1.1
Date: 3/27/2011 6:29:16 PM
Sheet: 2/2


ALUBUS[0..15]
IC8
10k
74LS541N
GND
DBUS[0..7]
IC1
74LS245N
/ALUHI2MEM
/MEM2ALUHI
IC6A
74LS08N
IC2
/ALULO2MEM
/MEM2ALULO
IC6B
IC3A
74LS244N
IC3B
IC7
ABUS[0..15]
RBUS[0..15]
IC4A
IC4B
IC5A
IC5B
/ENABUS
SV1
/LDMEM
MEMSEG
/RST
/FS
/IO
/ENMEM
IRQ[0..7]
+5V
OSC1
16.000MHz
IC10A
IC10B
74LS74N
IC11A
IC11B
IC11C
74LS32N
IC12A
IC12B
CLK0A
CLK0B
CLK0C
CLK0D
BUSCLKA
BUSCLKB
CLK1
/RST
CLK0
BUSCLK
CLK1
/RST is active for ~250ms
S1
IC9
MAX1232CPA
R18
4k
IC13A
IC13B
C9
C10
C11
C12
C13
C1
C2
C3
C4
C5
C6
C7
C8
100n
IC10P
IC11P
IC12P
IC13P
IC1P
IC2P
IC3P
IC4P
IC5P
IC6P
IC8P
IC7P
IC11D
IC6C
IC6D
R19
400
LED1
Clocks, reset, bus interface
Dawid Pilawa
(C) 2010, 2011
TITLE: cpu_interface
Document Number:
CPU.3
REV:
1.2
Date: 6/14/2011 10:30:23 PM
Sheet: 1/1


LBUS[0..15]
RBUS[0..15]
IC1
IC2
IC3
IC4
74LS181N
ALUOP0
ALUOP1
ALUOP2
ALUOP3
ALUMODE
/ALUCARRYIN
/ALUSHR
/ENALU
IC5
74S182N
/ALUCARRYIN
IC19B
74LS32N
IC19A
IC18C
74LS04N
IC19C
IC19D
IC11A
IC11B
IC12A
IC12B
IC13A
IC13B
IC14A
IC14B
74LS244N
GND
+5V
IC16A
IC16B
IC16C
IC16D
74LS02N
IC15A
IC15B
74LS21N
IC20A
74LS08N
IC9
74LS153N
ALU_N
ALU_Z
IC18D
IC8
IC10
IC7
74LS151N
ALU_V
IC18E
IC18F
IC6
IC18A
IC18B
ALU_C
IC1P
IC2P
IC3P
IC4P
IC5P
IC6P
IC7P
IC8P
IC9P
IC10P
IC11P
IC12P
IC13P
IC14P
IC15P
IC16P
IC17P
IC18P
IC19P
IC20P
100n
Arithmetic Logic Unit (ALU)
Dawid Pilawa
(C) 2010, 2011
TITLE: cpu_alu
Document Number:
CPU.4
REV: 1.1
Date: 3/27/2011 6:42:37 PM
Sheet: 1/1

/INC_MAR
/ENMAR
/LDMAR
/LDMARLO
/LDMARHI
CLK0B
/RST
ABUS[0..15]
ALUBUS[0..15]
/INCPC
/LDPC
/ENPC
/CNTSP
/LDSP
SP_DIR
/ENSP
/FS
CLK0C

IC1 IC2 IC3 IC4 IC5 IC6 IC7 IC8 IC12 IC13 IC14 IC15 IC16 IC17 IC18 IC19
74LS569

IC10 IC11
74LS157N

IC9A IC9B
74LS08N

IC9C IC9D
74LS08N

C19 IC9P
100n

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18
100n

+5V
GND

Registers (MAR,PC,KSP,SP)

Dawid Pilawa
(C) 2010, 2011

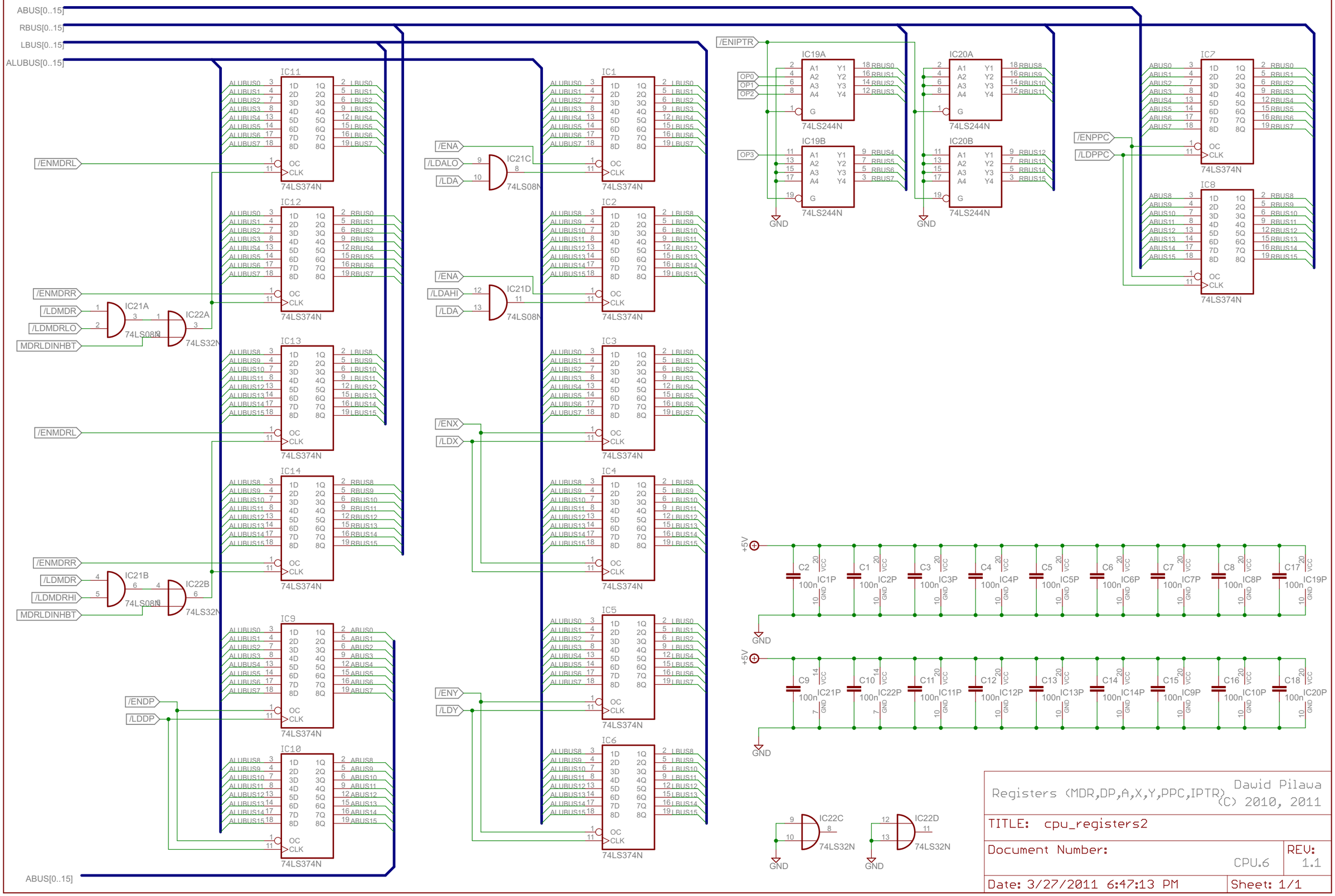
TITLE: cpu_registers1

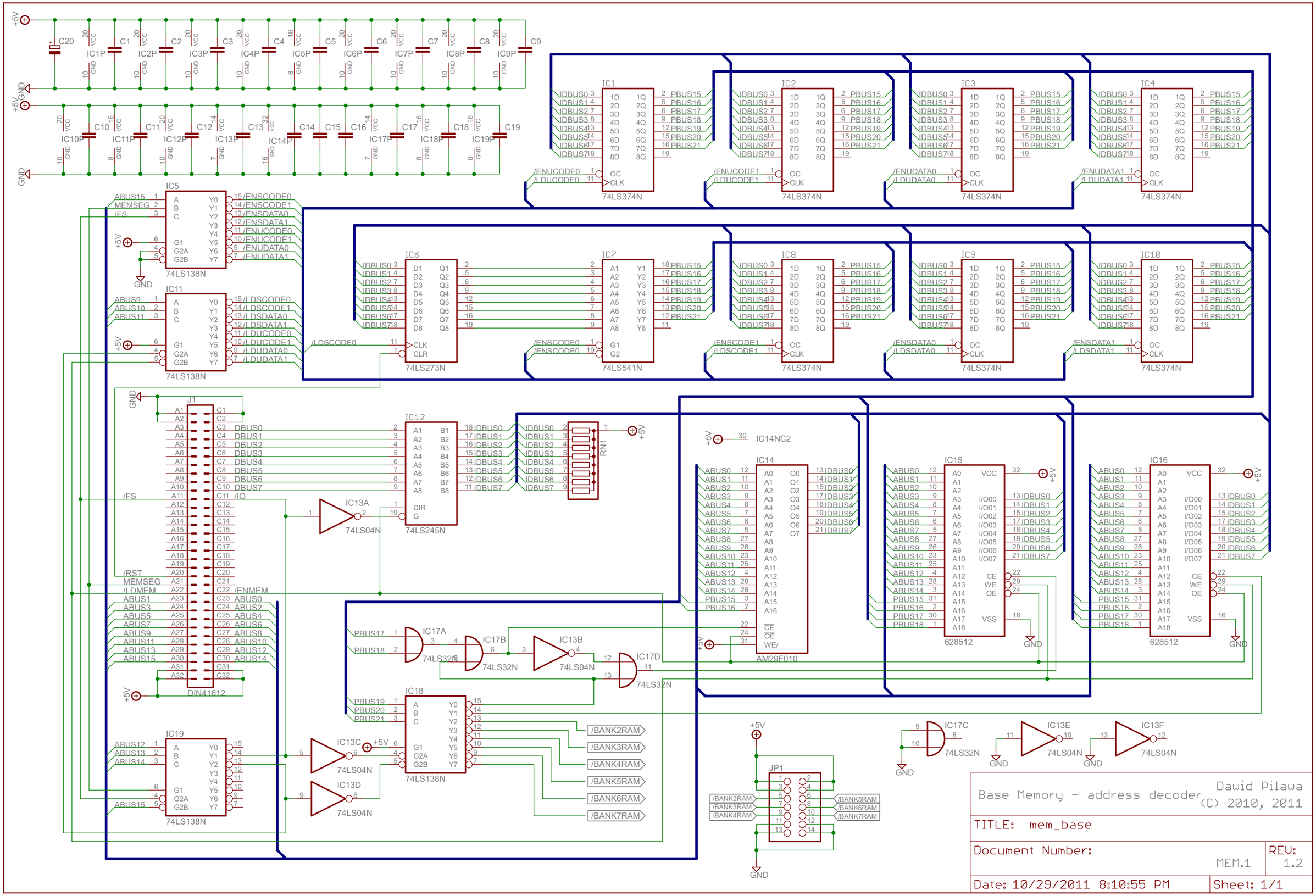
Document Number: CPU.5

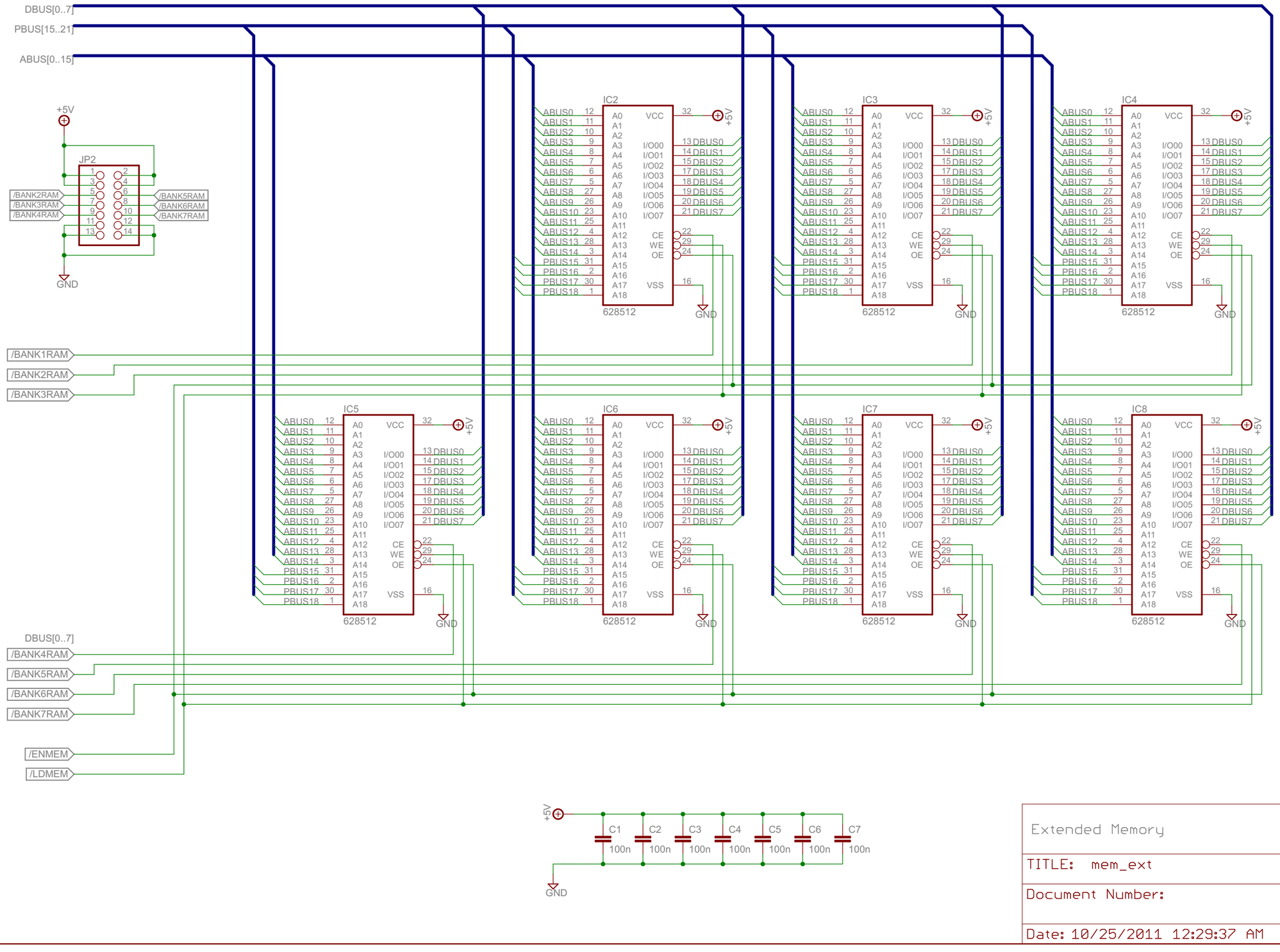
REV: 1.1

Date: 3/27/2011 6:46:15 PM

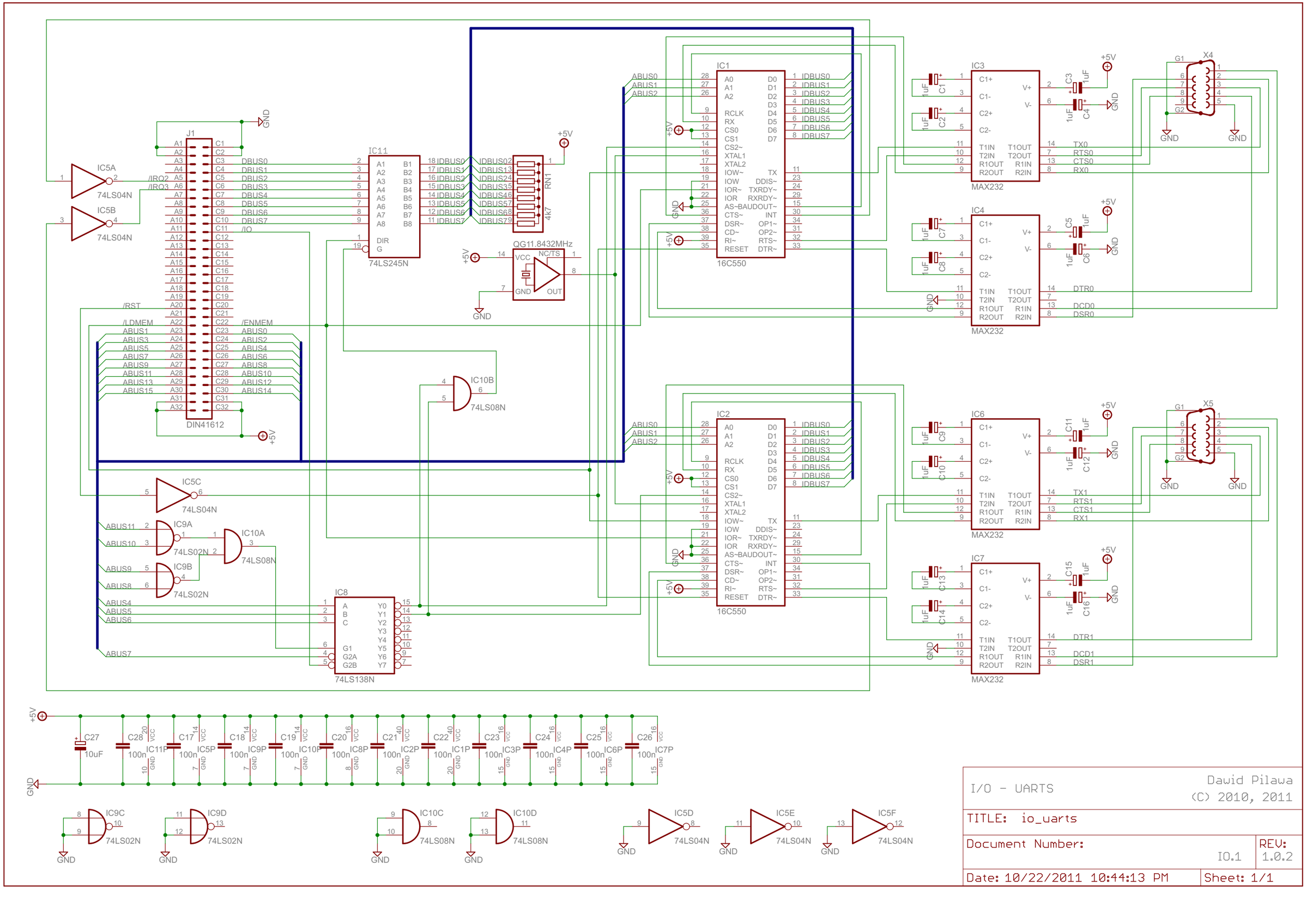
Sheet: 1/1


ABUS[0..15]
RBUS[0..15]
LBUS[0..15]
ALUBUS[0..15]
/ENMDRL
/ENMDRR
/LDMDR
/LDMDRLO
/LDMDRHI
MDRLDINHBT
/ENDP
/LDDP
/ENA
/LDALO
/LDAHI
/LDA
/ENX
/LDX
/ENY
/LDY
/ENIPTR
OP0
OP1
OP2
OP3
/ENPPC
/LDPPC
IC11
IC12
IC13
IC14
IC9
IC10
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC19A
IC19B
IC20A
IC20B
IC21A
IC21B
IC21C
IC21D
IC22A
IC22B
IC22C
IC22D
74LS374N
74LS08N
74LS32N
74LS244N
GND
+5V
C2 100n IC1P
C1 100n IC2P
C3 100n IC3P
C4 100n IC4P
C5 100n IC5P
C6 100n IC6P
C7 100n IC7P
C8 100n IC8P
C17 100n IC19P
C9 100n IC21P
C10 100n IC22P
C11 100n IC11P
C12 100n IC12P
C13 100n IC13P
C14 100n IC14P
C15 100n IC9P
C16 100n IC10P
C18 100n IC20P
Registers (MDR,DP,A,X,Y,PPC,IPTR)
Dawid Pilawa
(C) 2010, 2011
TITLE: cpu_registers2
Document Number: CPU.6
REV: 1.1
Date: 3/27/2011 6:47:13 PM
Sheet: 1/1


+5V
GND
C20
C1
C2
C3
C4
C5
C6
C7
C8
C9
IC1P
IC2P
IC3P
IC4P
IC5P
IC6P
IC7P
IC8P
IC9P
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
IC10P
IC11P
IC12P
IC13P
IC14P
IC17P
IC18P
IC19P
VCC
GND
IC1
IC2
IC3
IC4
74LS374N
/ENUCODE0
/LDUCODE0
/ENUCODE1
/LDUCODE1
/ENUDATA0
/LDUDATA0
/ENUDATA1
/LDUDATA1
IDBUS0
IDBUS1
IDBUS2
IDBUS3
IDBUS4
IDBUS5
IDBUS6
IDBUS7
PBUS15
PBUS16
PBUS17
PBUS18
PBUS19
PBUS20
PBUS21
IC5
74LS138N
ABUS15
MEMSEG
/FS
/ENSCODE0
/ENSCODE1
/ENSDATA0
/ENSDATA1
/ENUCODE0
/ENUCODE1
/ENUDATA0
/ENUDATA1
IC11
ABUS9
ABUS10
ABUS11
/LDSCODE0
/LDSCODE1
/LDSDATA0
/LDSDATA1
/LDUCODE0
/LDUCODE1
/LDUDATA0
/LDUDATA1
IC6
IC7
IC8
IC9
IC10
74LS273N
74LS541N
74LS374N
/ENSCODE0
/ENSCODE1
/ENSDATA0
/ENSDATA1
J1
DIN41612
DBUS0
DBUS1
DBUS2
DBUS3
DBUS4
DBUS5
DBUS6
DBUS7
/IO
/RST
/I DMEM
/ENMEM
ABUS0
ABUS1
ABUS2
ABUS3
ABUS4
ABUS5
ABUS6
ABUS7
ABUS8
ABUS9
ABUS10
ABUS11
ABUS12
ABUS13
ABUS14
ABUS15
IC12
74LS245N
RN1
IC13A
IC13B
IC13C
IC13D
74LS04N
IC14NC2
IC14
AM29F010
IC15
IC16
628512
IC17A
IC17B
IC17C
IC17D
74LS32N
IC18
74LS138N
/BANK2RAM
/BANK3RAM
/BANK4RAM
/BANK5RAM
/BANK6RAM
/BANK7RAM
JP1
IC13E
IC13F
Dawid Pilawa
Base Memory - address decoder
(C) 2010, 2011
TITLE: mem_base
Document Number:
MEM.1
REV:
1.2
Date: 10/29/2011 8:10:55 PM
Sheet: 1/1



Extended Memory	Dawid Pilawa (C) 2010, 2011
TITLE: mem_ext	
Document Number: MEM.2	REV: 1.2
Date: 10/25/2011 12:29:37 AM	Sheet: 1/1


J1
DIN41612
GND
+5V
/RST
/LDMEM
/ENMEM
/IO
/IRQ2
/IRQ3
DBUS0
DBUS1
DBUS2
DBUS3
DBUS4
DBUS5
DBUS6
DBUS7
ABUS0
ABUS1
ABUS2
ABUS3
ABUS4
ABUS5
ABUS6
ABUS7
ABUS8
ABUS9
ABUS10
ABUS11
ABUS12
ABUS13
ABUS14
ABUS15
IC5A
74LS04N
IC5B
74LS04N
IC5C
74LS04N
IC11
74LS245N
IDBUS0
IDBUS1
IDBUS2
IDBUS3
IDBUS4
IDBUS5
IDBUS6
IDBUS7
IDBUS02
IDBUS13
IDBUS24
IDBUS35
IDBUS46
IDBUS57
IDBUS68
IDBUS79
RN1
4k7
QG11.8432MHz
NC/TS
VCC
GND
OUT
IC10B
74LS08N
IC9A
74LS02N
IC10A
74LS08N
IC9B
74LS02N
IC8
74LS138N
IC1
16C550
IC2
16C550
IC3
MAX232
IC4
MAX232
IC6
MAX232
IC7
MAX232
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
1uF
X4
X5
G1
G2
TX0
RTS0
CTS0
RX0
DTR0
DCD0
DSR0
TX1
RTS1
CTS1
RX1
DTR1
DCD1
DSR1
C27
10uF
100n
IC9C
74LS02N
IC9D
74LS02N
IC10C
74LS08N
IC10D
74LS08N
IC5D
74LS04N
IC5E
74LS04N
IC5F
74LS04N
I/O - UARTS
Dawid Pilawa
(C) 2010, 2011
TITLE: io_uarts
Document Number:
IO.1
REV:
1.0.2
Date: 10/22/2011 10:44:13 PM
Sheet: 1/1