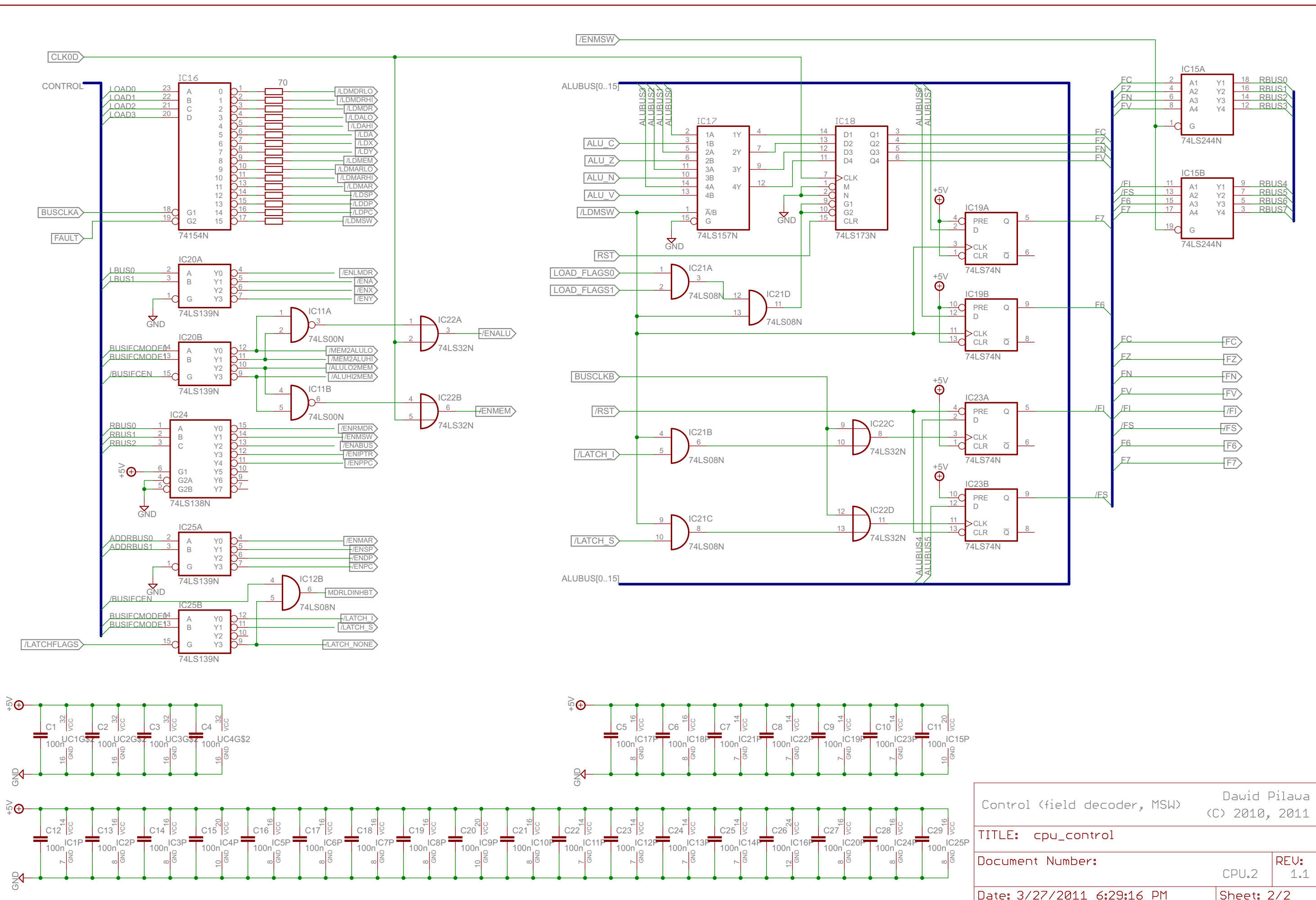


Control (microcode sequencer) Dawid Pilawa	
(C) 2010, 2011	
TITLE: cpu_control	
Document Number:	REU: 1.1
CPU.1	
Date: 3/27/2011 6:29:16 PM	Sheet: 1/2

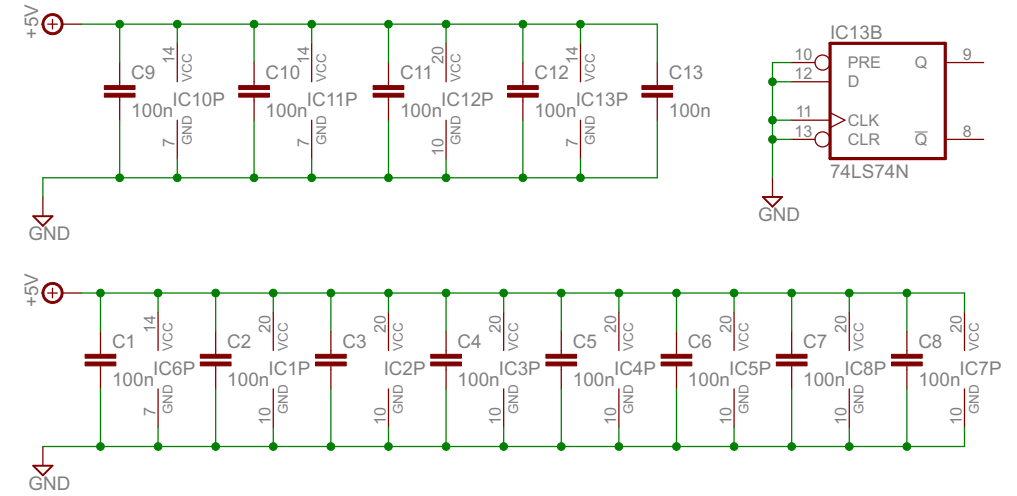
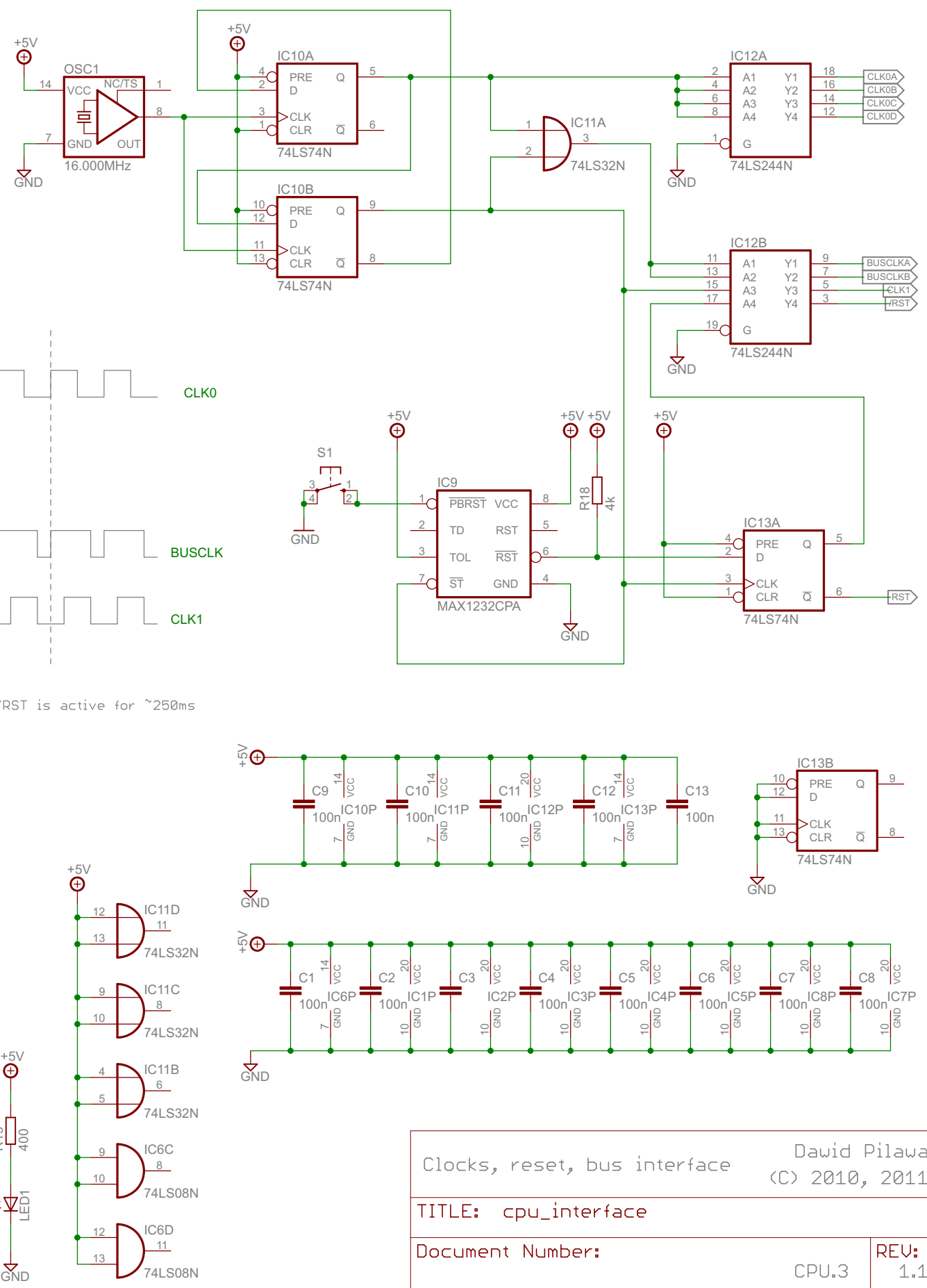
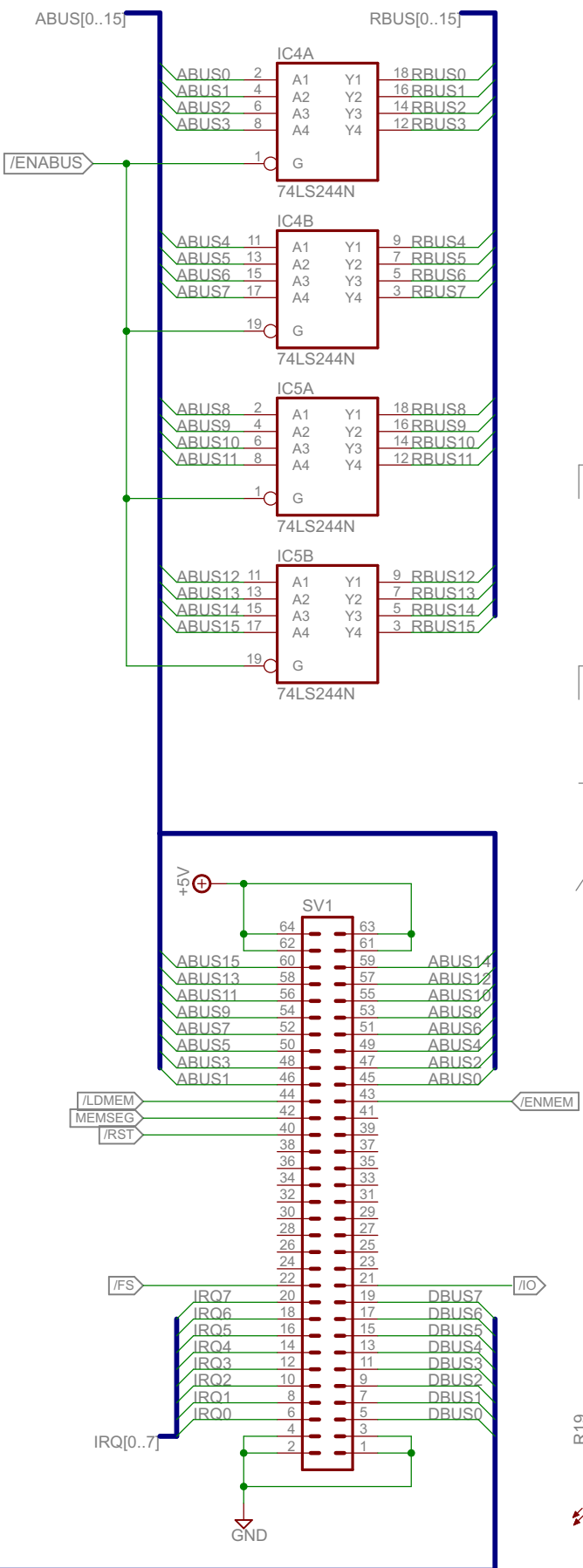
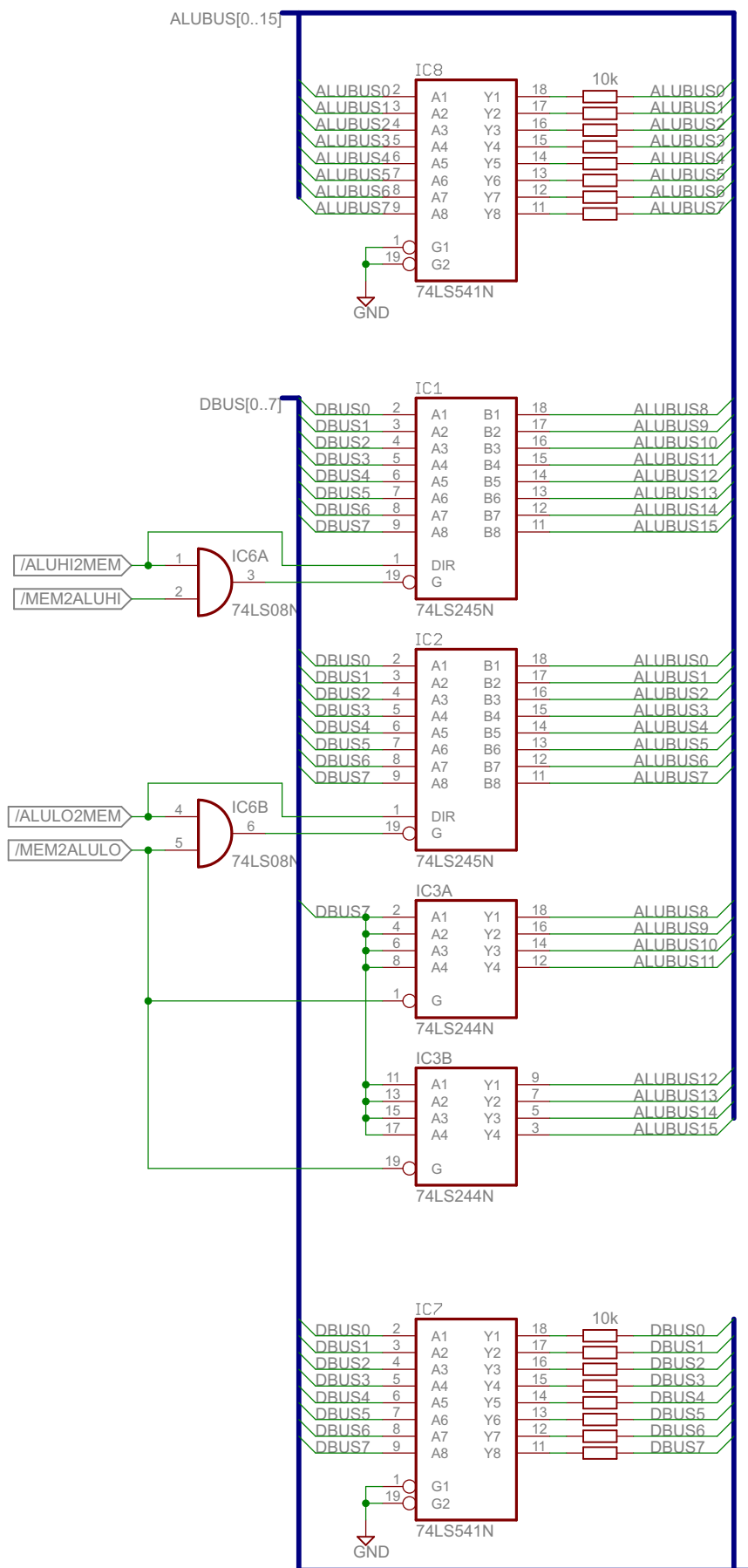


Control (field decoder, MSW) Dawid Pilawa
(C) 2010, 2011

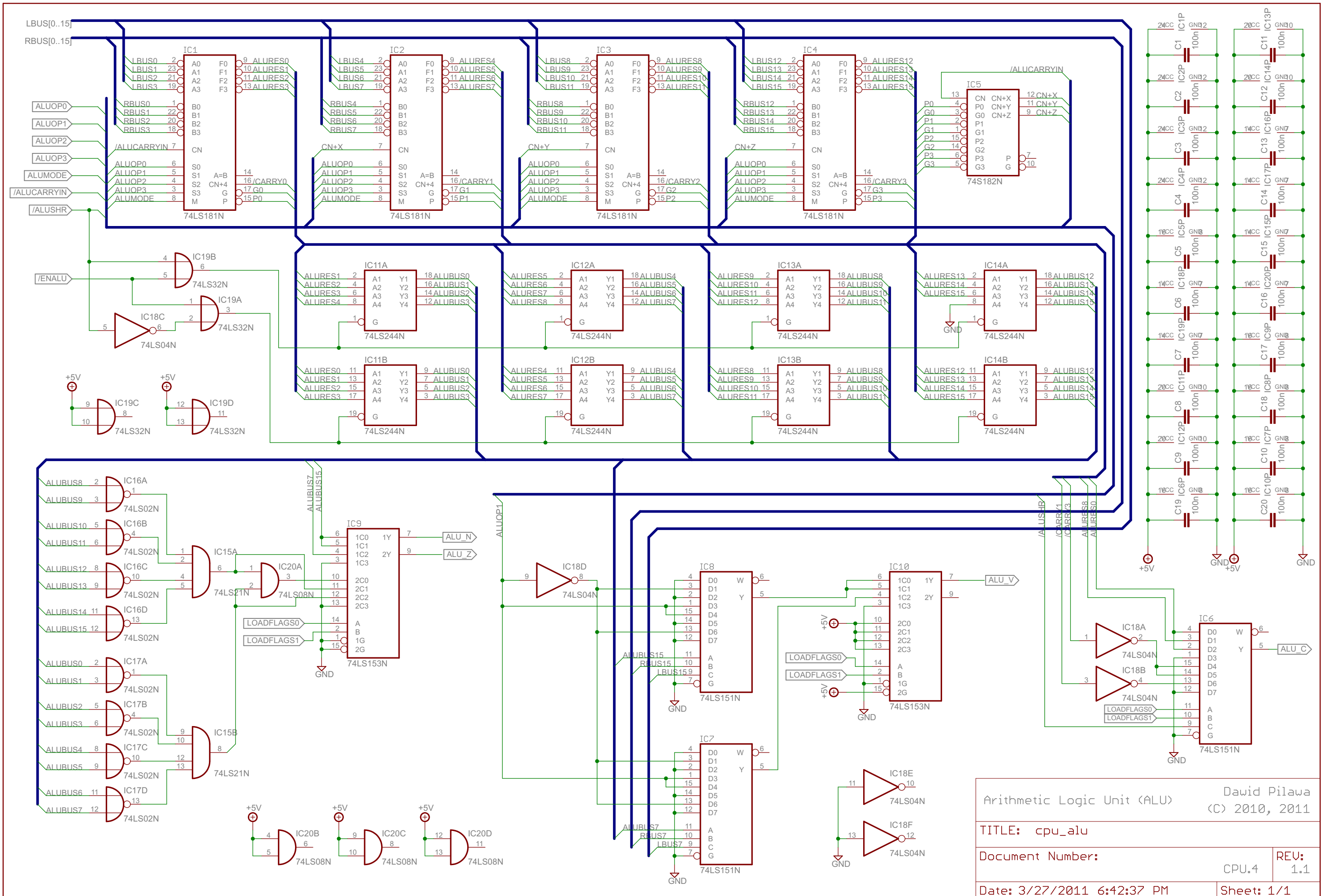
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Document Number: REV: 1.1

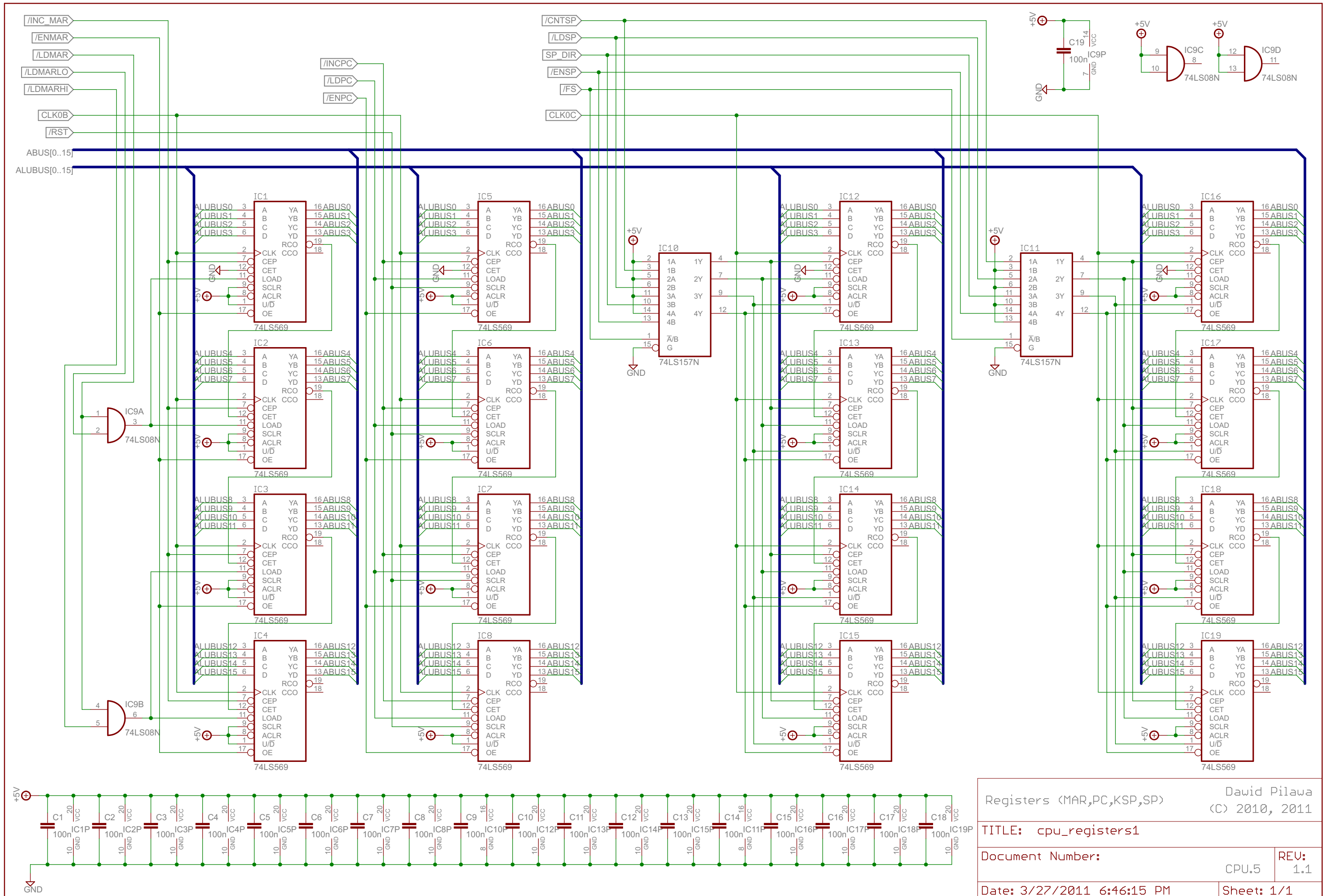
Date: 3/27/2011 6:29:16 PM CPU.2 Sheet: 2/2



Clocks, reset, bus interface		Dawid Pilawa	
		(C) 2010, 2011	
TITLE: cpu_interface			
Document Number:		CPU.3	
Date: 3/27/2011 6:39:06 PM		REU: 1.1	
		Sheet: 1/1	



Arithmetic Logic Unit (ALU)		Dawid Pilawa	
TITLE: cpu_alu		(C) 2010, 2011	
Document Number:		CPU.4	REV: 1.1
Date: 3/27/2011 6:42:37 PM		Sheet: 1/1	

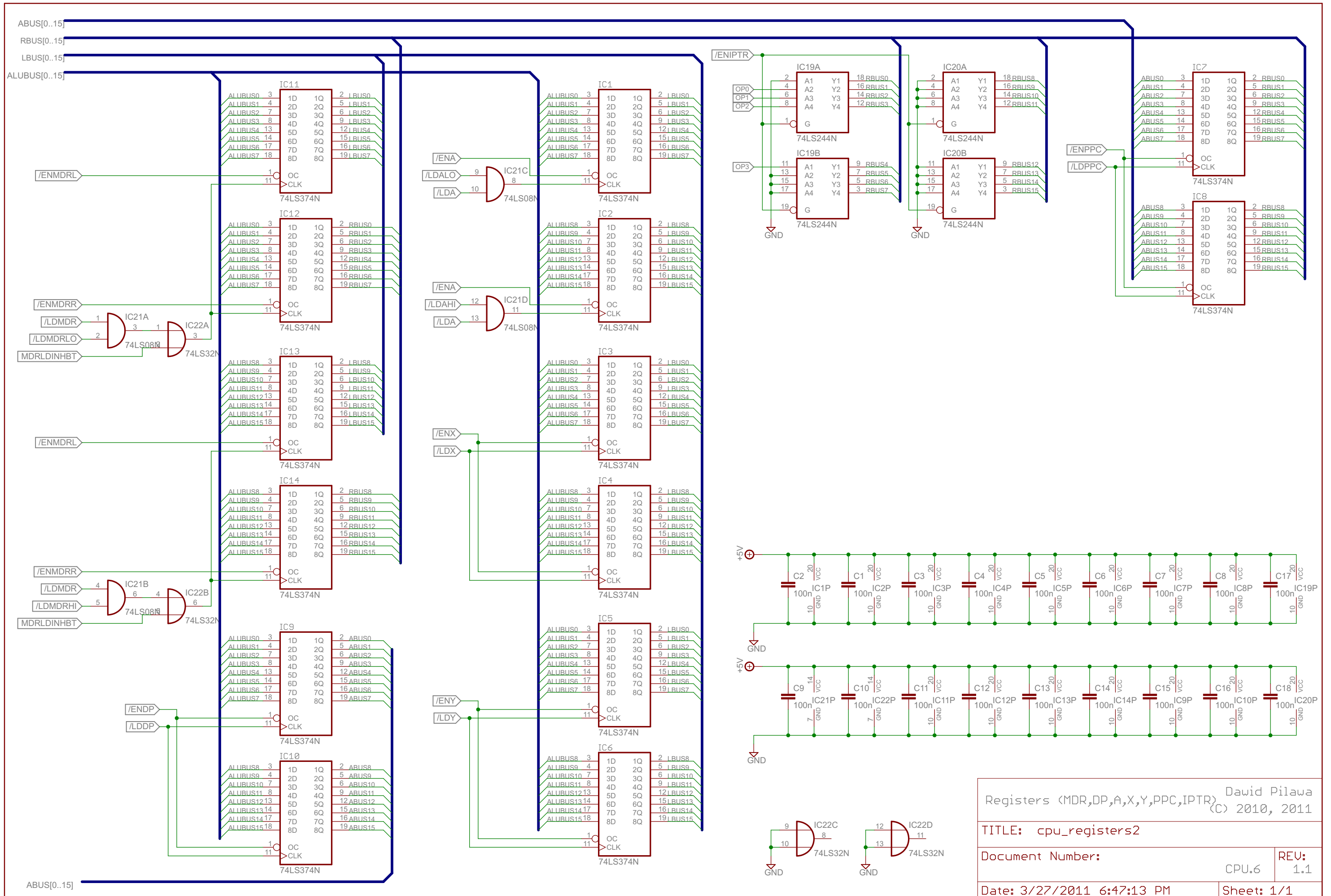


Registers (MAR,PC,KSP,SP) Dawid Pilawa
(C) 2010, 2011

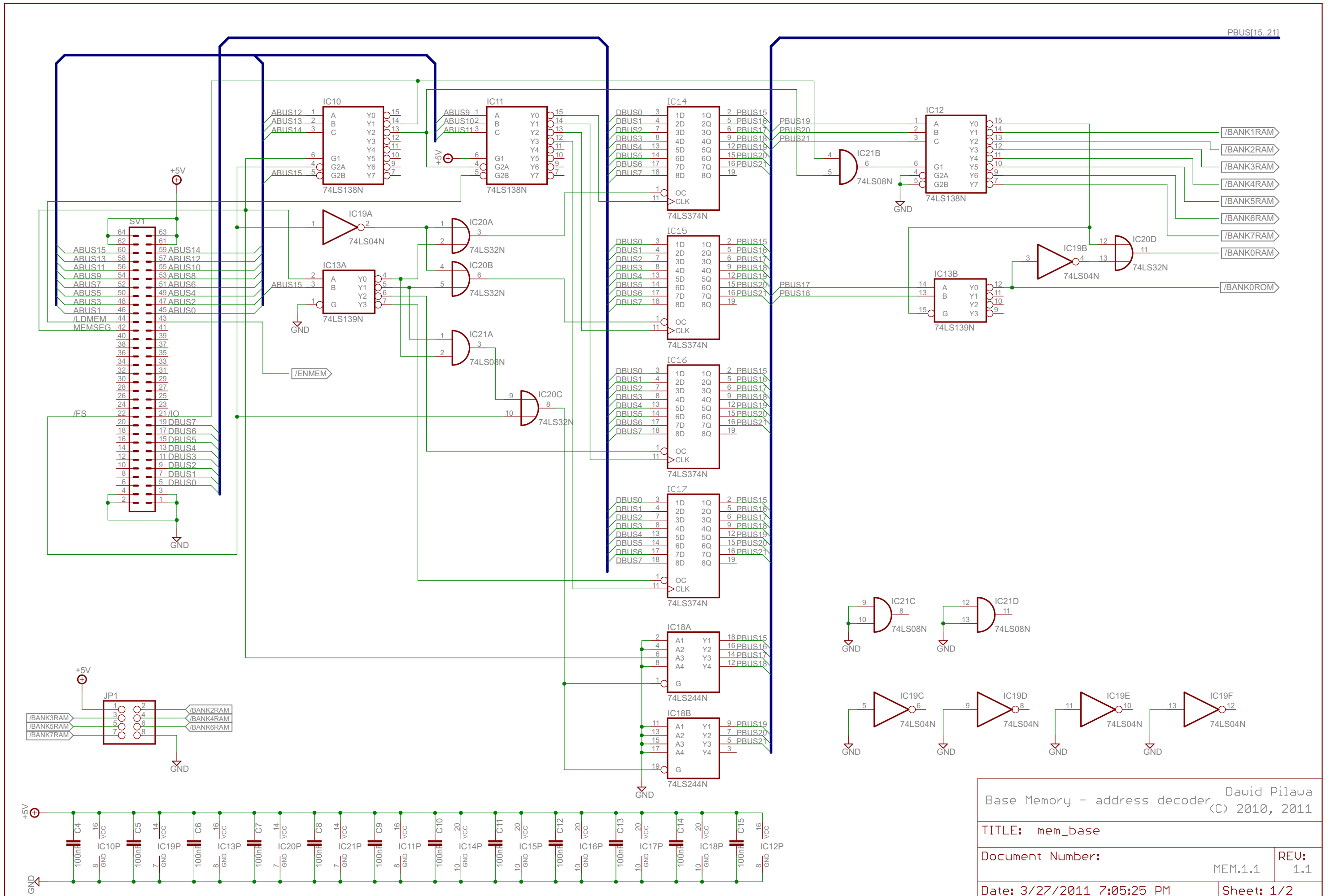
TITLE: `cpu_registers1`

Document Number: REV: 1.1

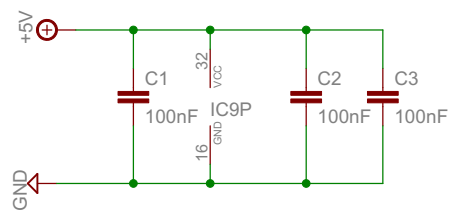
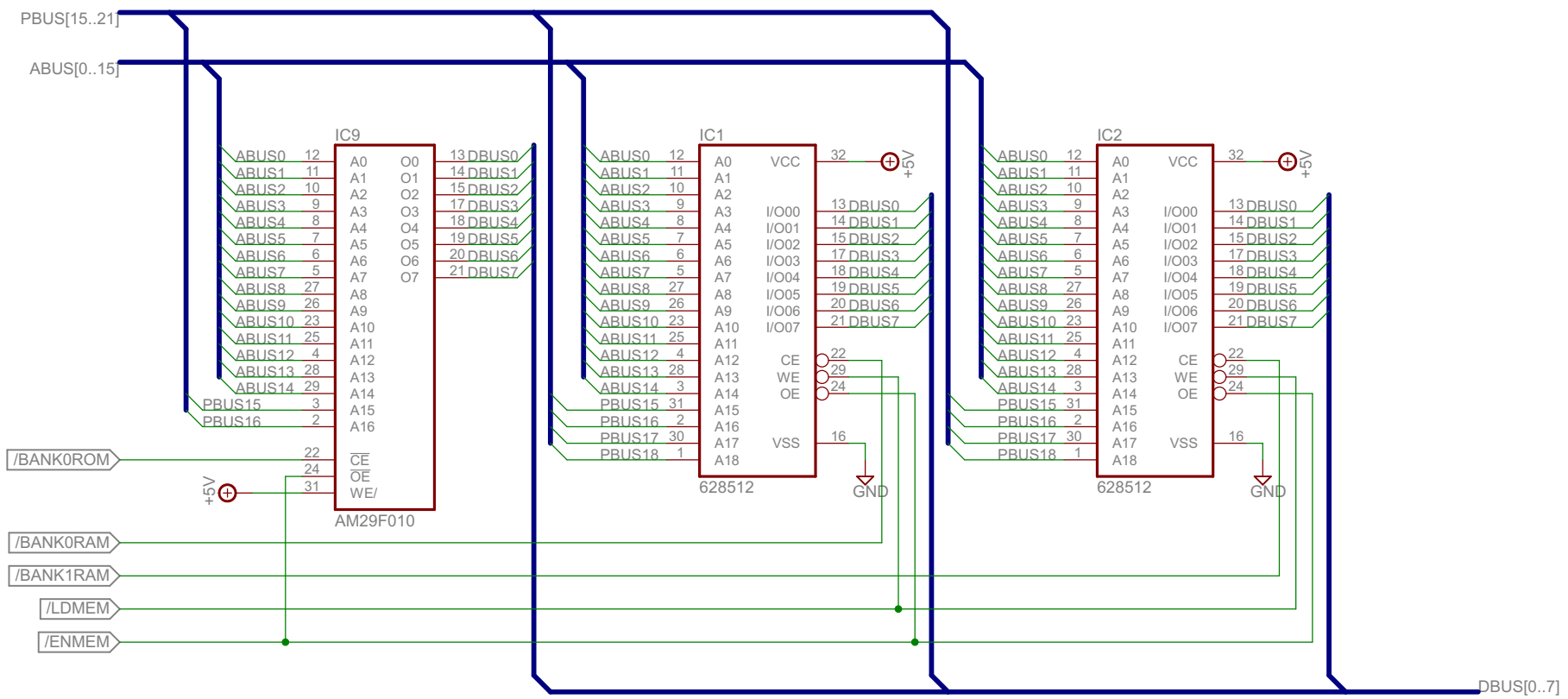
Date: 3/27/2011 6:46:15 PM CPU.5
Sheet: 1/1



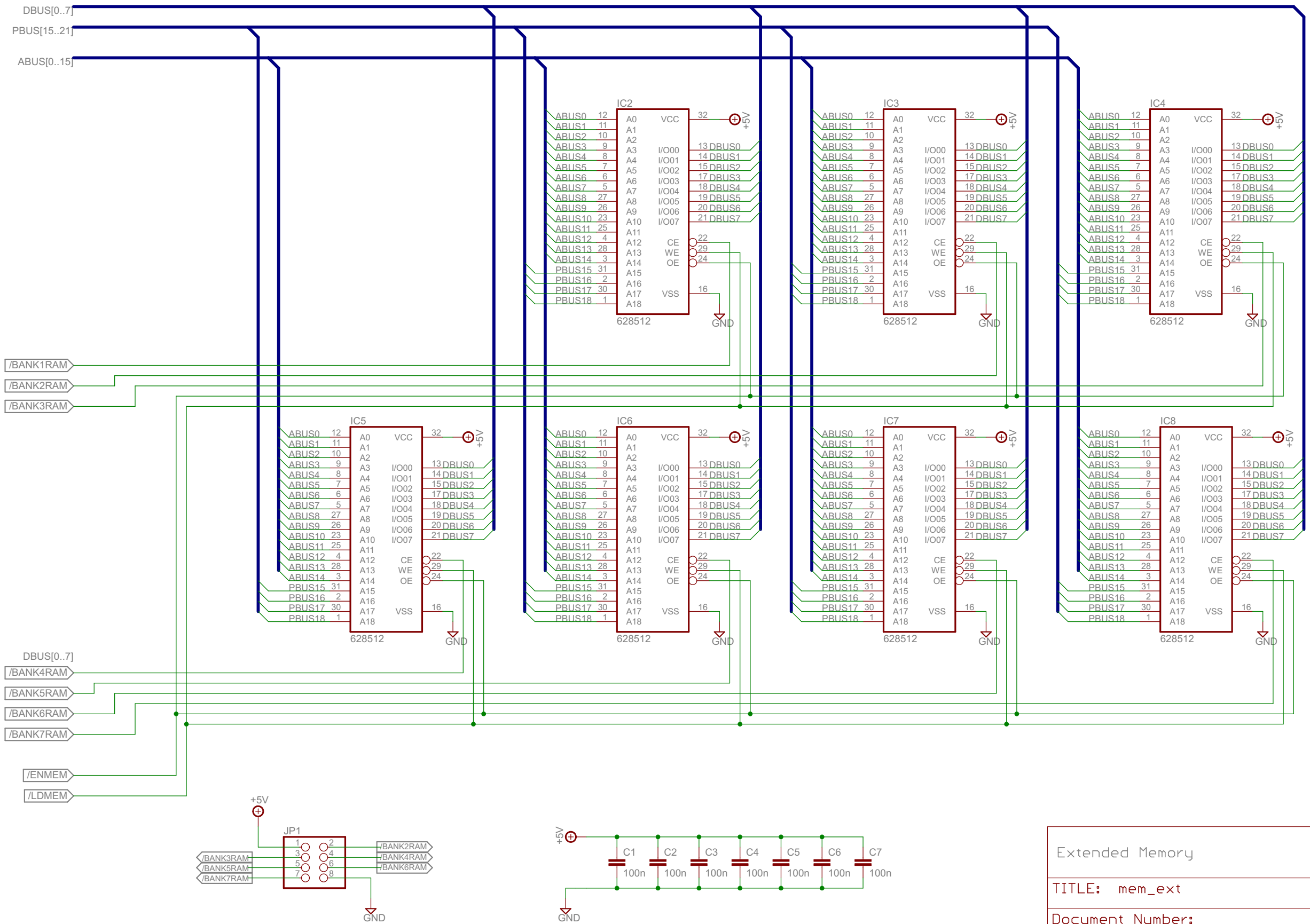
Registers (MDR,DP,A,X,Y,PPC,IPTR) Dawid Pilawa
 (C) 2010, 2011
 TITLE: cpu_registers2
 Document Number: CPU.6 REV: 1.1
 Date: 3/27/2011 6:47:13 PM Sheet: 1/1



Base Memory - address decoder		Dawid Pilawa (C) 2010, 2011	
TITLE: mem_base			
Document Number:		MEM.1.1	REV: 1.1
Date: 3/27/2011 7:05:25 PM		Sheet: 1/2	



Base Memory - ROM and RAM		Dawid Pilawa (C) 2010, 1011	
TITLE: mem_base			
Document Number:		MEM.1.2	REV: 1.1
Date: 3/27/2011 7:05:25 PM		Sheet: 2/2	



Extended Memory		Dawid Pilawa (C) 2010, 2011	
TITLE: mem_ext			
Document Number:		MEM.2	REU: 1.1
Date: 3/27/2011 7:18:53 PM		Sheet: 1/1	