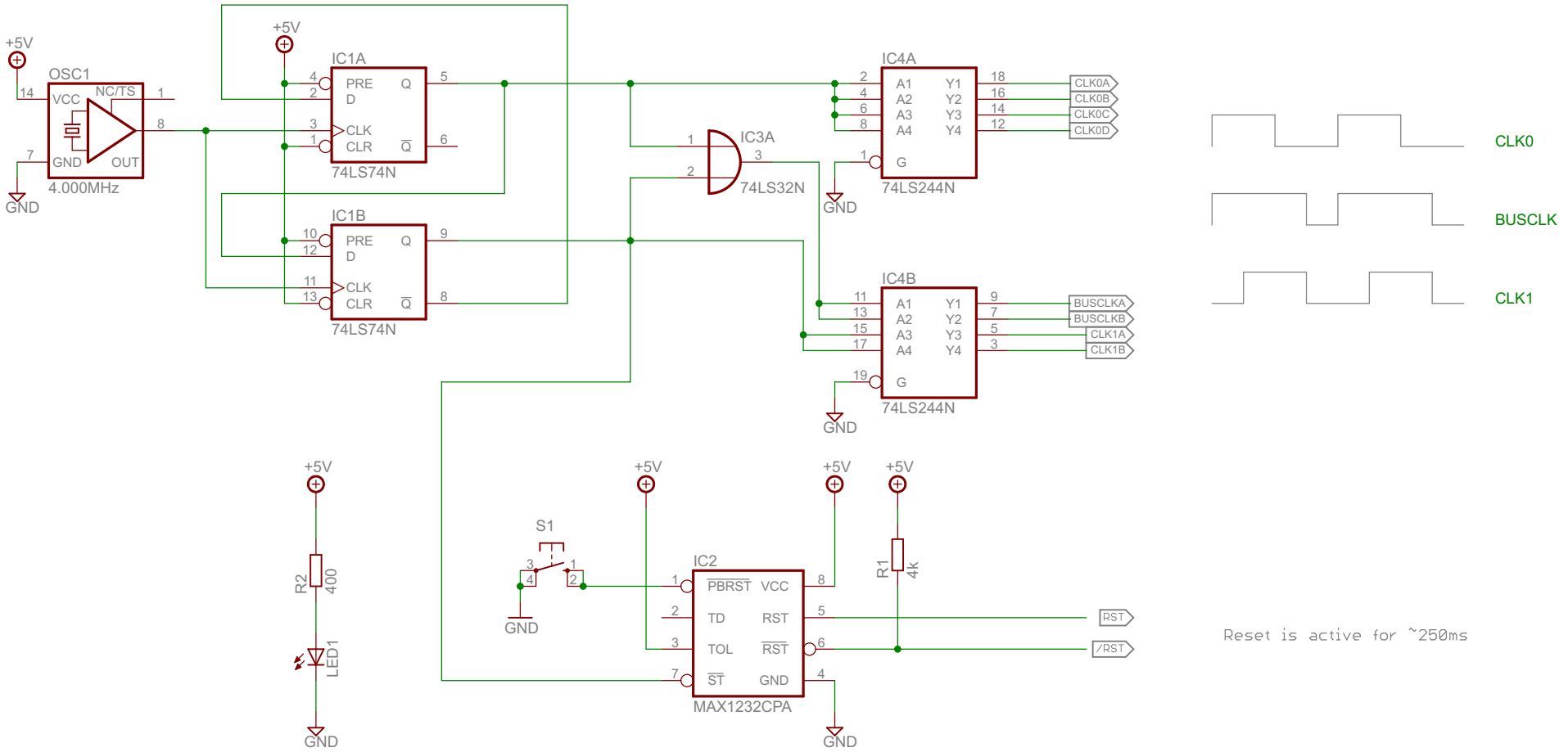
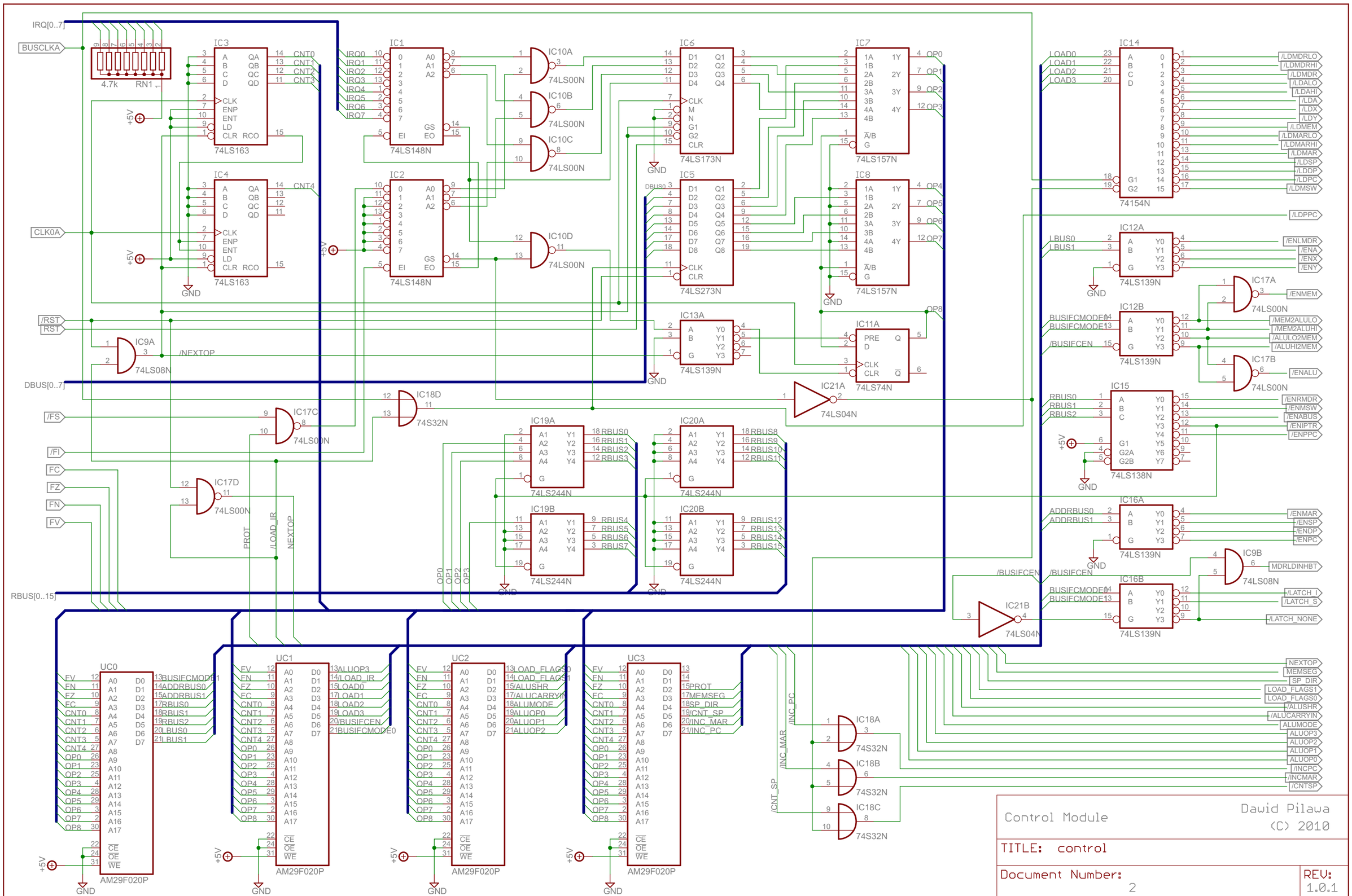
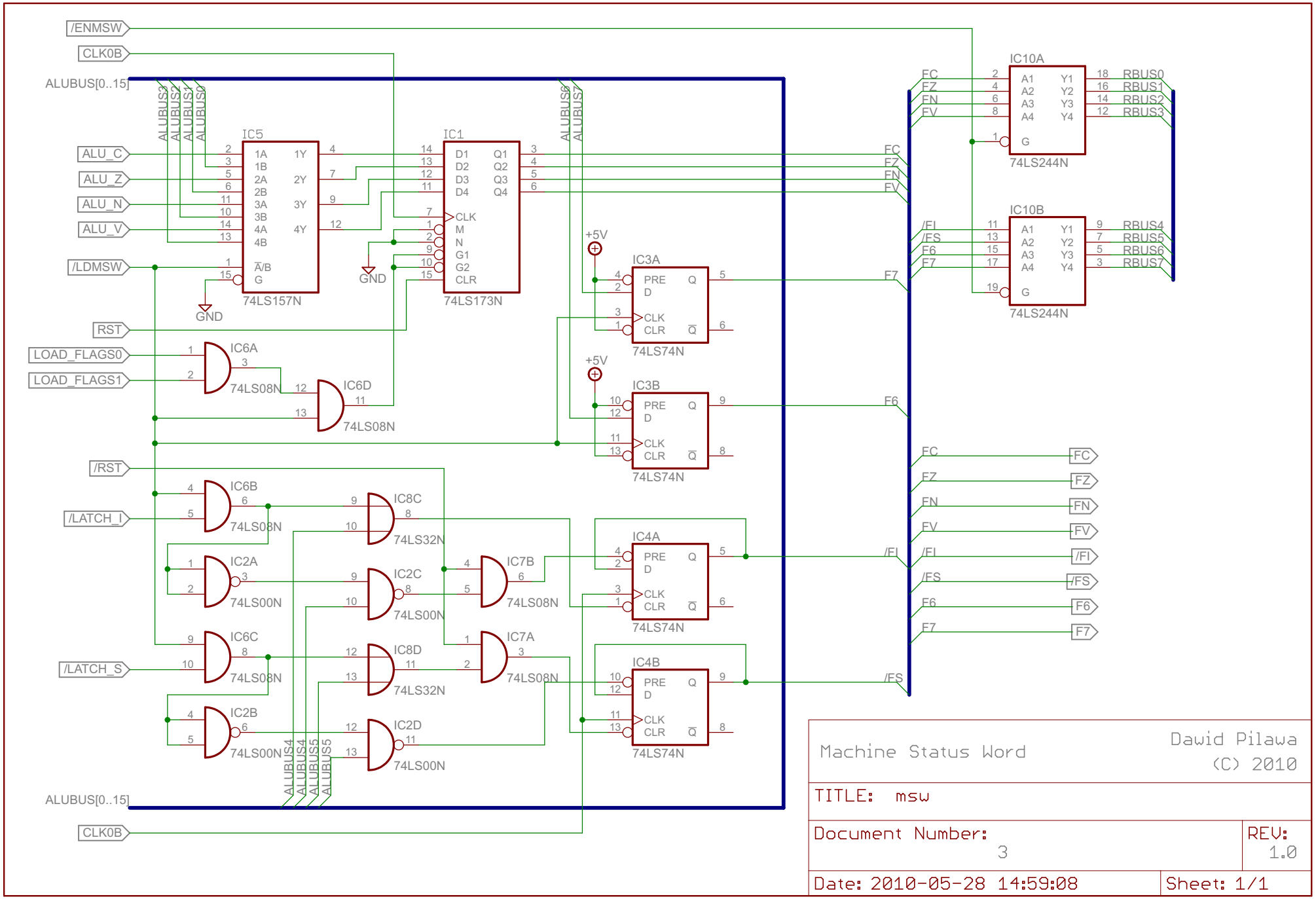
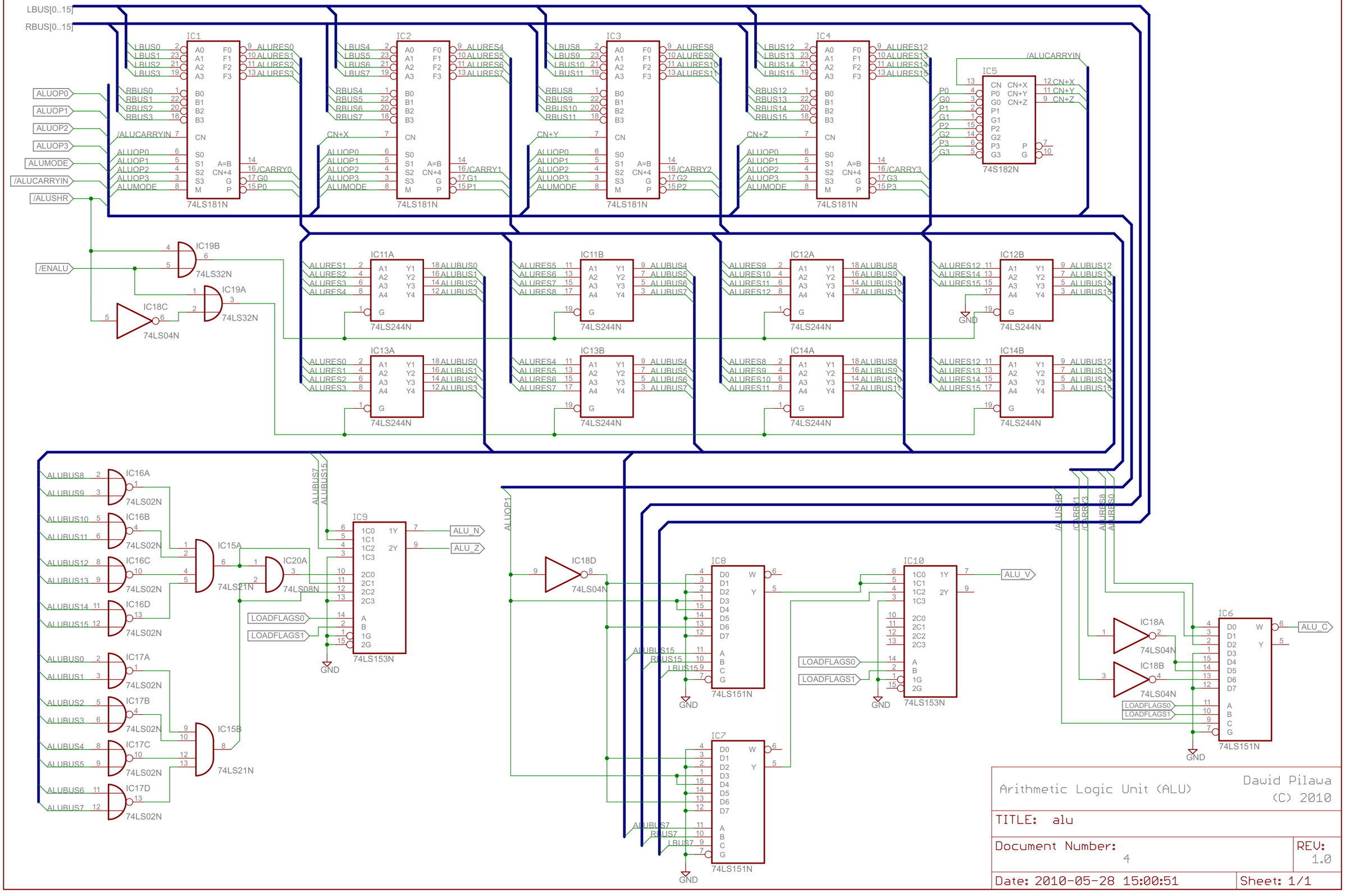
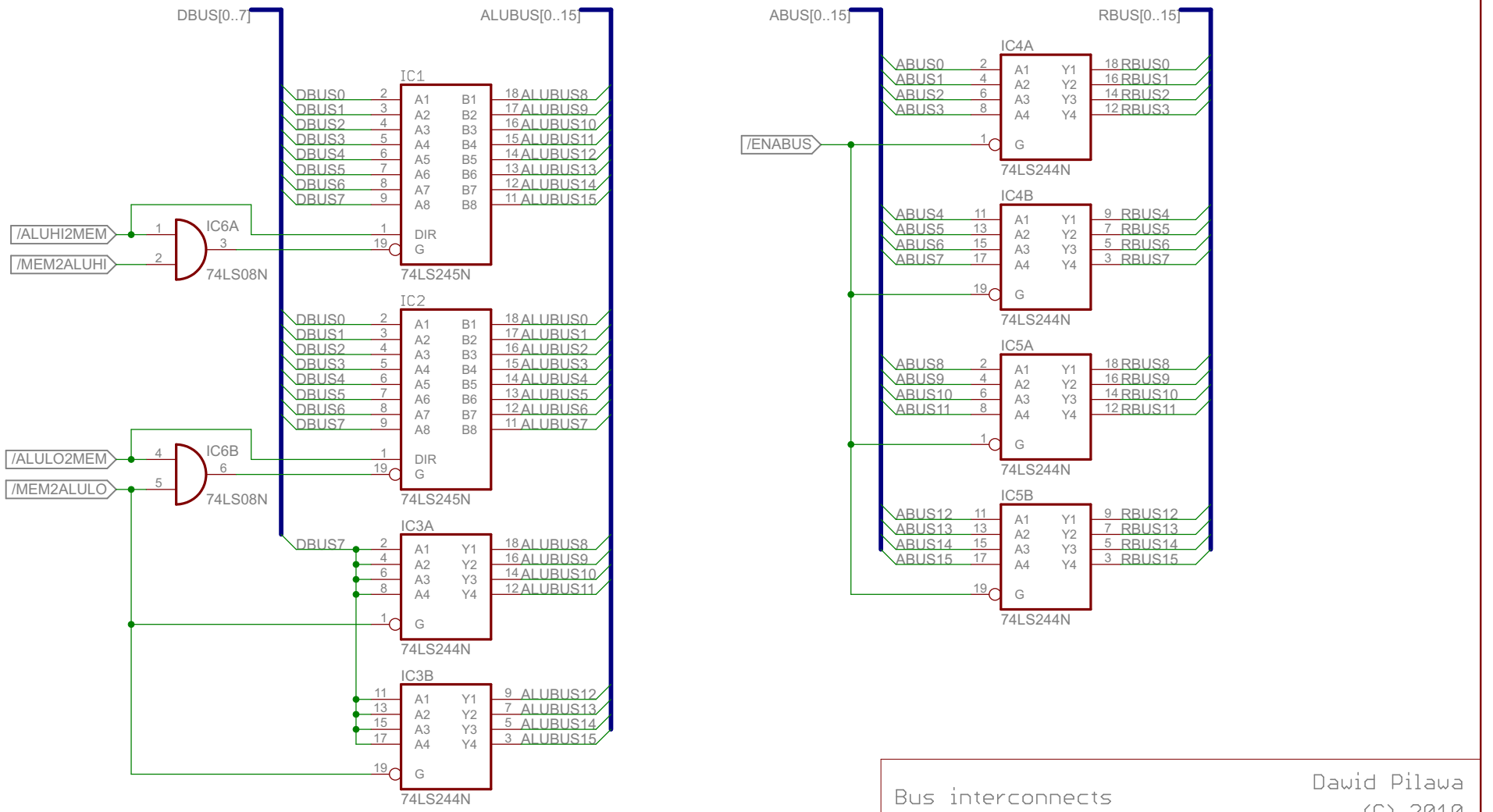


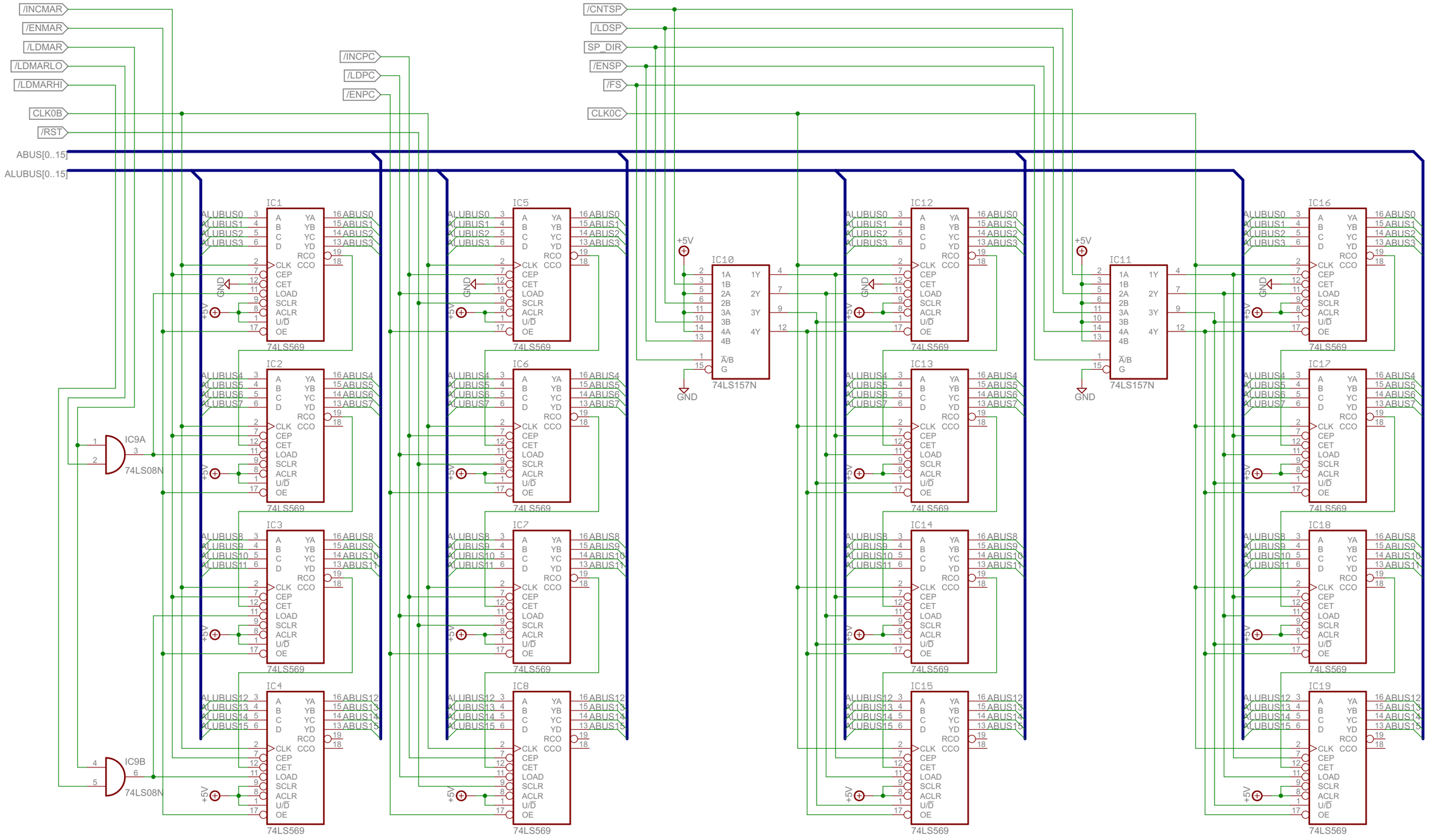
Clock generation and reset	Dawid Pilawa (C) 2010
TITLE: clkrst	
Document Number: 1	REV: 1.0.1
Date: 2010-06-14 09:08:58	Sheet: 1/1

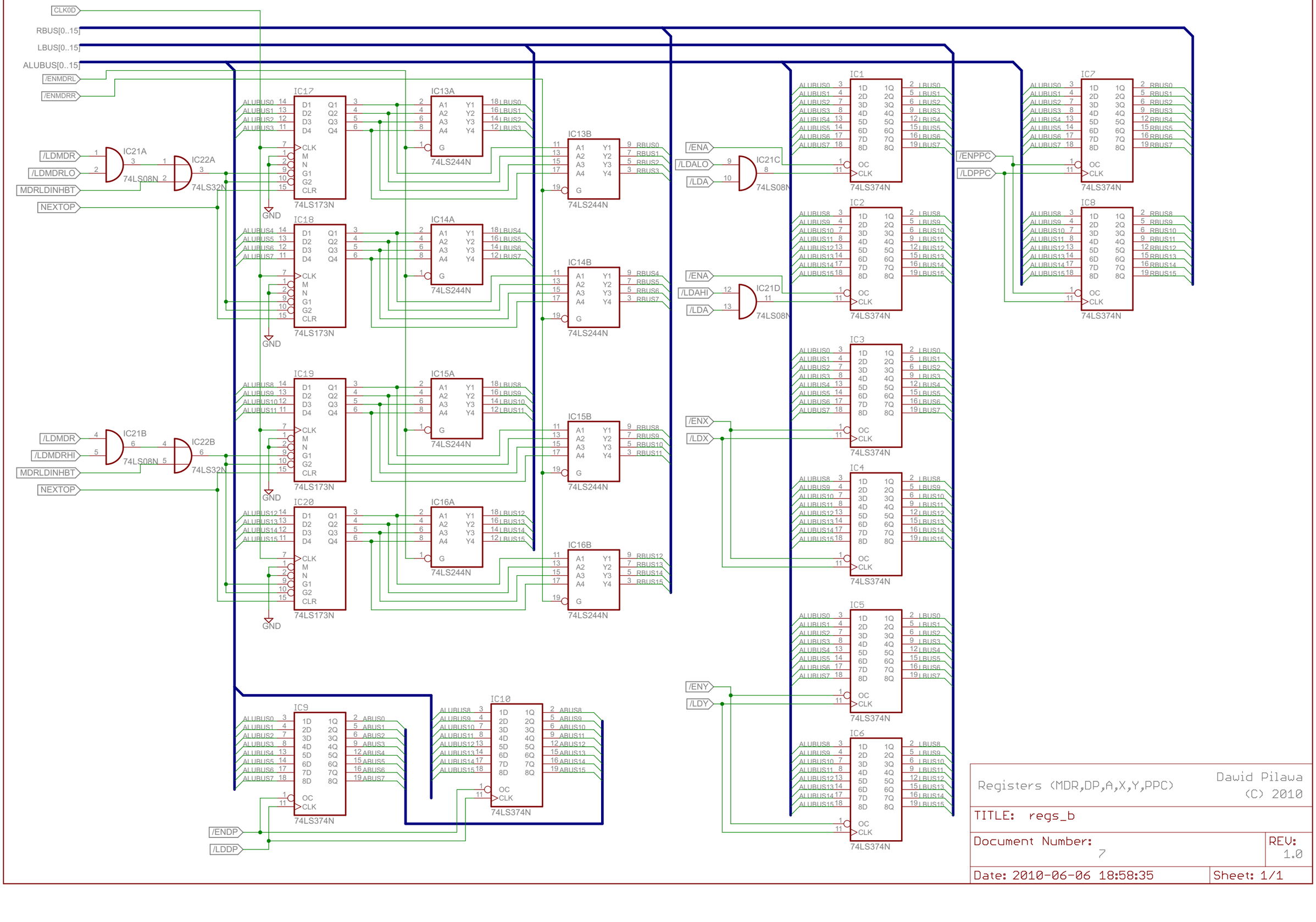

IRQ[0..7]
BUSCLKA
4.7k
RN1
IC3
74LS163
IC4
74LS163
CLK0A
+5V
GND
/RST
RST
IC9A
74LS08N
/NEXTOP
DBUS[0..7]
IC1
74LS148N
IC2
74LS148N
IC10A
IC10B
IC10C
IC10D
74LS00N
IC6
74LS173N
IC5
74LS273N
DBUS0
IC7
74LS157N
IC8
74LS157N
OP0
OP1
OP2
OP3
OP4
OP5
OP6
OP7
OP8
IC13A
74LS139N
IC11A
74LS74N
IC21A
74LS04N
IC14
74154N
LOAD0
LOAD1
LOAD2
LOAD3
/LDMDRLO
/LDMDRHI
/LDMDR
/LDALO
/LDAHI
/LDA
/LDX
/LDY
/LDMEM
/LDMARLO
/LDMARHI
/LDMAR
/LDSP
/LDDP
/LDPC
/LDMSW
/LDPPC
IC12A
LBUS0
LBUS1
/ENLMDR
/ENA
/ENX
/ENY
IC12B
BUSIFCMODE0
BUSIFCMODE1
/BUSIFCEN
/ENMEM
/MEM2ALULO
/MEM2ALUHI
/ALULO2MEM
/ALUHI2MEM
IC17A
IC17B
74LS00N
/ENALU
IC15
74LS138N
RBUS0
RBUS1
RBUS2
/ENRMDR
/ENMSW
/ENABUS
/ENIPTR
/ENPPC
IC16A
ADDRBUS0
ADDRBUS1
/ENMAR
/ENSP
/ENDP
/ENPC
IC9B
MDRLDINHBT
IC16B
/LATCH_I
/LATCH_S
/LATCH_NONE
/FS
/FI
FC
FZ
FN
FV
IC17C
IC17D
74LS00N
IC18D
74S32N
PROT
/LOAD_IR
NEXTOP
IC19A
IC19B
IC20A
IC20B
74LS244N
RBUS[0..15]
UC0
UC1
UC2
UC3
AM29F020P
BUSIFCMODE1
ADDRBUS0
ADDRBUS1
RBUS0
RBUS1
RBUS2
LBUS0
LBUS1
ALUOP3
/LOAD_IR
LOAD0
LOAD1
LOAD2
LOAD3
/BUSIFCEN
BUSIFCMODE0
LOAD_FLAGS0
LOAD_FLAGS1
/ALUSHR
ALUMODE
ALUOP2
ALUOP1
ALUOP0
PROT
MEMSEG
SP_DIR
/CNT_SP
/INC_MAR
/INC_PC
IC18A
IC18B
IC18C
NEXTOP
MEMSEG
SP_DIR
LOAD_FLAGS1
LOAD_FLAGS0
/ALUSHR
/ALUCARRYIN
ALUMODE
ALUOP3
ALUOP2
ALUOP1
ALUOP0
/INCPC
/INCMAR
/CNTSP
Control Module
Dawid Pilawa
(C) 2010
TITLE: control
Document Number: 2
REV: 1.0.1
Date: 2010-07-07 09:50:29
Sheet: 1/1


/ENMSW
CLK0B
ALUBUS[0..15]
ALU_C
ALU_Z
ALU_N
ALU_V
/LDMSW
RST
LOAD_FLAGS0
LOAD_FLAGS1
/RST
/LATCH_I
/LATCH_S
IC5
74LS157N
IC1
74LS173N
GND
+5V
IC3A
IC3B
74LS74N
IC6A
IC6D
74LS08N
IC6B
IC6C
IC2A
IC2B
74LS00N
IC8C
IC8D
74LS32N
IC7B
IC7A
IC4A
IC4B
IC2C
IC2D
FC
FZ
FN
FV
/FI
/FS
F6
F7
IC10A
IC10B
74LS244N
RBUS0
RBUS1
RBUS2
RBUS3
RBUS4
RBUS5
RBUS6
RBUS7
Machine Status Word
Dawid Pilawa
(C) 2010
TITLE: msw
Document Number: 3
REV: 1.0
Date: 2010-05-28 14:59:08
Sheet: 1/1


LBUS[0..15]
RBUS[0..15]
IC1
IC2
IC3
IC4
IC5
74LS181N
74LS182N
ALUOP0
ALUOP1
ALUOP2
ALUOP3
ALUMODE
/ALUCARRYIN
/ALUSHR
/ENALU
/CARRY0
/CARRY1
/CARRY2
/CARRY3
P0
P1
P2
P3
G0
G1
G2
G3
CN+X
CN+Y
CN+Z
IC19B
IC19A
IC18C
74LS32N
74LS04N
IC11A
IC11B
IC12A
IC12B
IC13A
IC13B
IC14A
IC14B
74LS244N
GND
IC16A
IC16B
IC16C
IC16D
IC17A
IC17B
IC17C
IC17D
74LS02N
IC15A
IC15B
74LS21N
IC20A
74LS08N
IC9
74LS153N
LOADFLAGS0
LOADFLAGS1
ALU_N
ALU_Z
IC18D
IC8
IC7
74LS151N
IC10
ALU_V
IC18A
IC18B
IC6
ALU_C
Arithmetic Logic Unit (ALU)
Dawid Pilawa
(C) 2010
TITLE: alu
Document Number: 4
REV: 1.0
Date: 2010-05-28 15:00:51
Sheet: 1/1


DBUS[0..7]
ALUBUS[0..15]
IC1
DBUS0 2
DBUS1 3
DBUS2 4
DBUS3 5
DBUS4 6
DBUS5 7
DBUS6 8
DBUS7 9
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
18 ALUBUS8
17 ALUBUS9
16 ALUBUS10
15 ALUBUS11
14 ALUBUS12
13 ALUBUS13
12 ALUBUS14
11 ALUBUS15
DIR 1
G 19
74LS245N
/ALUHI2MEM 1
/MEM2ALUHI 2
IC6A
3
74LS08N
IC2
18 ALUBUS0
17 ALUBUS1
16 ALUBUS2
15 ALUBUS3
14 ALUBUS4
13 ALUBUS5
12 ALUBUS6
11 ALUBUS7
/ALULO2MEM 4
/MEM2ALULO 5
IC6B
6
74LS08N
IC3A
Y1 Y2 Y3 Y4
18 ALUBUS8
16 ALUBUS9
14 ALUBUS10
12 ALUBUS11
G 1
74LS244N
IC3B
9 ALUBUS12
7 ALUBUS13
5 ALUBUS14
3 ALUBUS15
G 19
74LS244N
ABUS[0..15]
RBUS[0..15]
/ENABUS
IC4A
ABUS0 2
ABUS1 4
ABUS2 6
ABUS3 8
18 RBUS0
16 RBUS1
14 RBUS2
12 RBUS3
G 1
74LS244N
IC4B
ABUS4 11
ABUS5 13
ABUS6 15
ABUS7 17
9 RBUS4
7 RBUS5
5 RBUS6
3 RBUS7
G 19
74LS244N
IC5A
ABUS8 2
ABUS9 4
ABUS10 6
ABUS11 8
18 RBUS8
16 RBUS9
14 RBUS10
12 RBUS11
G 1
74LS244N
IC5B
ABUS12 11
ABUS13 13
ABUS14 15
ABUS15 17
9 RBUS12
7 RBUS13
5 RBUS14
3 RBUS15
G 19
74LS244N
Bus interconnects
Dawid Pilawa
(C) 2010
TITLE: busic
Document Number:
5
REV:
1.0
Date: 2010-05-28 14:59:46
Sheet: 1/1


/INCMAR
/ENMAR
/LDMAR
/LDMARLO
/LDMARHI
CLK0B
/RST
ABUS[0..15]
ALUBUS[0..15]
/INCPC
/LDPC
/ENPC
/CNTSP
/LDSP
SP_DIR
/ENSP
/FS
CLK0C
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9A
IC9B
74LS08N
IC10
IC11
IC12
IC13
IC14
IC15
IC16
IC17
IC18
IC19
74LS569
74LS157N
+5V
GND
Registers (MAR,PC,KSP,SP)
Dawid Pilawa
(C) 2010
TITLE: regs_a
Document Number: 6
REV: 1.0
Date: 2010-05-28 14:59:00
Sheet: 1/1


CLK0D
RBUS[0..15]
LBUS[0..15]
ALUBUS[0..15]
/ENMDRL
/ENMDRR
/LDMDR
/LDMDRLO
MDRLDINHBT
NEXTOP
/LDMDRHI
/ENDP
/LDDP
/ENA
/LDALO
/LDA
/LDAHI
/ENX
/LDX
/ENY
/LDY
/ENPPC
/LDPPC
IC21A
IC21B
IC21C
IC21D
IC22A
IC22B
74LS08N
74LS32N
IC17
IC18
IC19
IC20
74LS173N
IC13A
IC13B
IC14A
IC14B
IC15A
IC15B
IC16A
IC16B
74LS244N
IC9
IC10
74LS374N
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
GND
Registers (MDR,DP,A,X,Y,PPC)
Dawid Pilawa
(C) 2010
TITLE: regs_b
Document Number: 7
REV: 1.0
Date: 2010-06-06 18:58:35
Sheet: 1/1

PBUS[15..21]

IC10 74LS138N — A=ABUS12, B=ABUS13, C=ABUS14, G1=+5V, G2A=ABUS15, G2B=GND
IC11 74LS138N — A=ABUS9, B=ABUS10, C=ABUS11, G1=+5V, G2A=+5V, G2B=GND

SV1 — ABUS15 ABUS13 ABUS11 ABUS9 ABUS7 ABUS5 ABUS3 ABUS1 /LDMEM MEMSEG ABUS14 ABUS12 ABUS10 ABUS8 ABUS6 ABUS4 ABUS2 ABUS0 /IO DBUS7 DBUS6 DBUS5 DBUS4 DBUS3 DBUS2 DBUS1 DBUS0 /FS +5V GND

IC19A 74LS04N
IC13A 74LS139N — A=ABUS15, G=GND
IC20A 74LS32N
IC20B 74LS32N
IC21A 74LS08N
IC20C 74LS32N
/ENMEM

IC14 74LS374N — DBUS0..7 → PBUS15..PBUS21
IC15 74LS374N — DBUS0..7 → PBUS15..PBUS21
IC16 74LS374N — DBUS0..7 → PBUS15..PBUS21
IC17 74LS374N — DBUS0..7 → PBUS15..PBUS21
OC=GND, CLK=/ENMEM

IC18A 74LS244N — A1..A4 = PBUS15..PBUS18, G=GND
IC18B 74LS244N — A1..A3 = PBUS19..PBUS21, G=GND

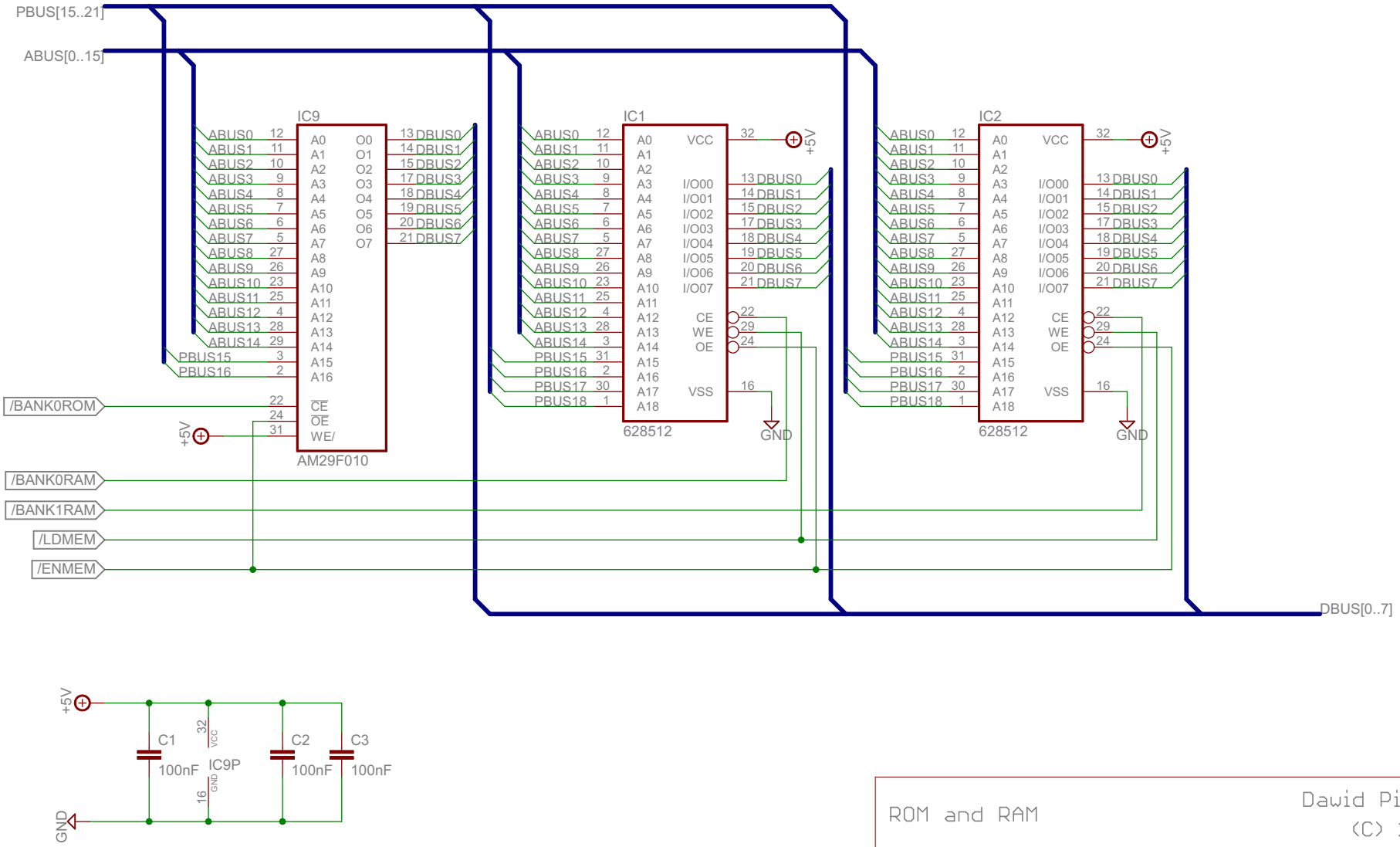
PBUS19 PBUS20 PBUS21 → IC21B 74LS08N (other input GND)
PBUS17 PBUS18 → IC13B 74LS139N

IC12 74LS138N — A=PBUS19, B=PBUS20, C=PBUS21, G1=IC21B, G2A=GND, G2B=IC13B
IC19B 74LS04N
IC20D 74LS32N

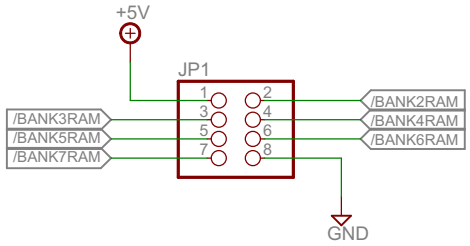
/BANK1RAM
/BANK2RAM
/BANK3RAM
/BANK4RAM
/BANK5RAM
/BANK6RAM
/BANK7RAM
/BANK0RAM
/BANK0ROM

+5V / GND
C4 100nF IC10P
C5 100nF IC19P
C6 100nF IC13P
C7 100nF IC20P
C8 100nF IC21P
C9 100nF IC11P
C10 100nF IC14P
C11 100nF IC15P
C12 100nF IC16P
C13 100nF IC17P
C14 100nF IC18P
C15 100nF IC12P

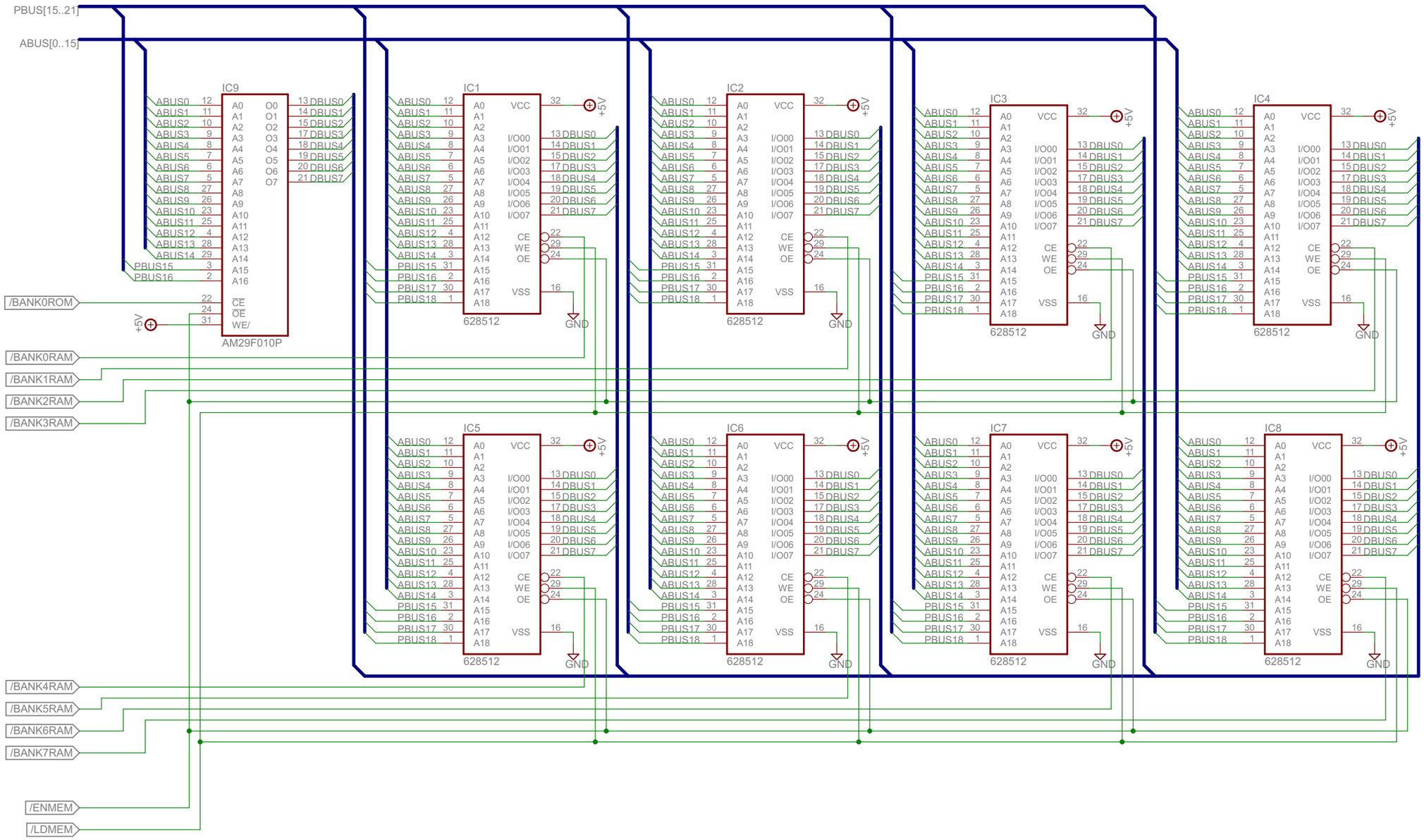
Address decoder	Dawid Pilawa (C) 2010
TITLE: mem_base	
Document Number: 8	REV: 1.0.1
Date: 2010-07-27 23:08:51	Sheet: 1/3



ROM and RAM	Dawid Pilawa (C) 2010
TITLE: mem_base	
Document Number: 8	REV: 1.0.1
Date: 2010-07-27 23:08:51	Sheet: 2/3



Extension board connector	Dawid Pilawa (C) 2010
TITLE: mem_base	
Document Number: 8	REV: 1.0.1
Date: 2010-07-27 23:08:51	Sheet: 3/3



Memory Unit (ROM and RAM)		Dawid Pilawa (C) 2010
TITLE: mem_ext		
Document Number: 9		REV: 1.0
Date: 2010-07-13 15:27:38	Sheet: 1/1	